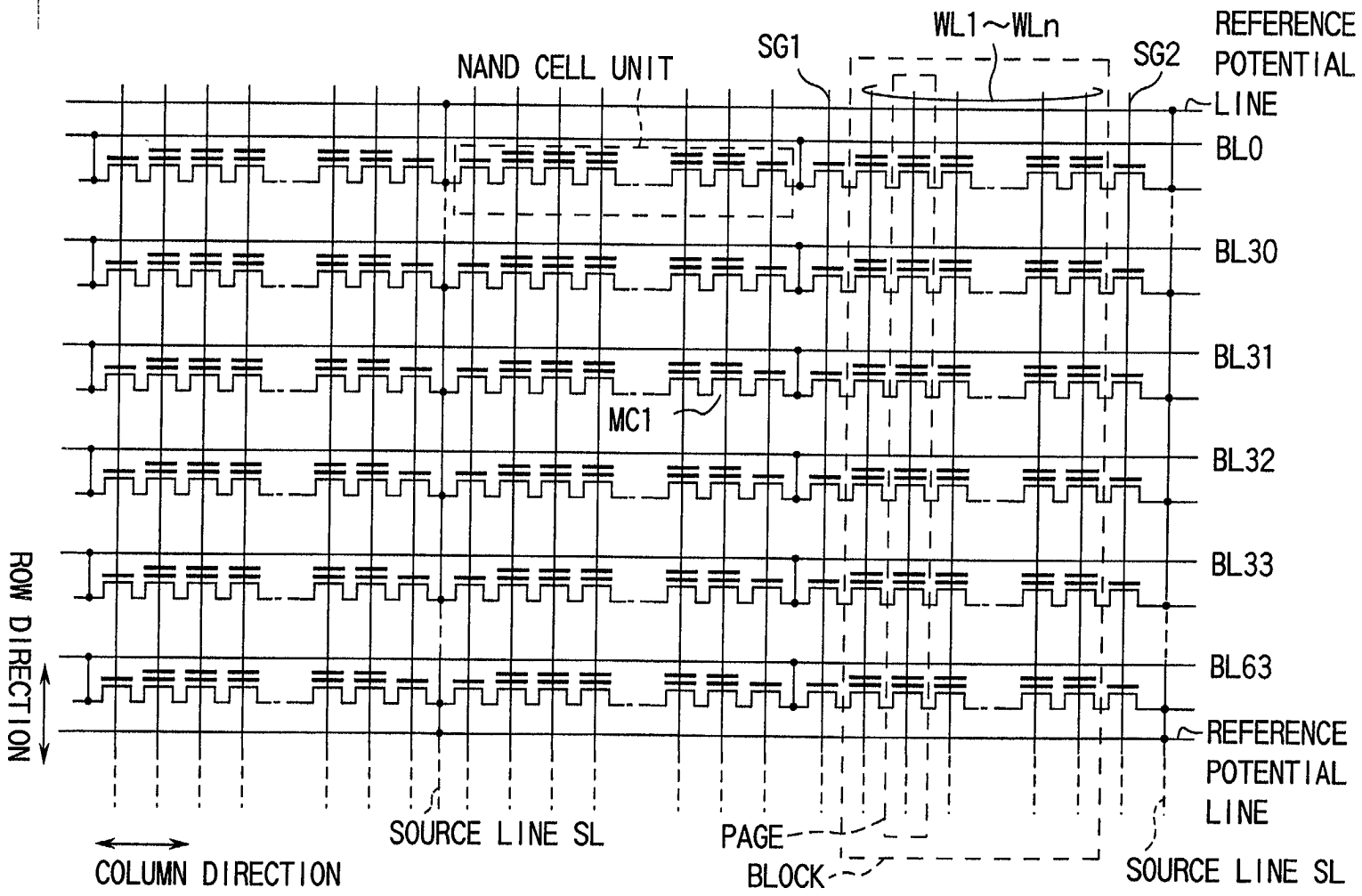


FIG. 1 PRIOR ART

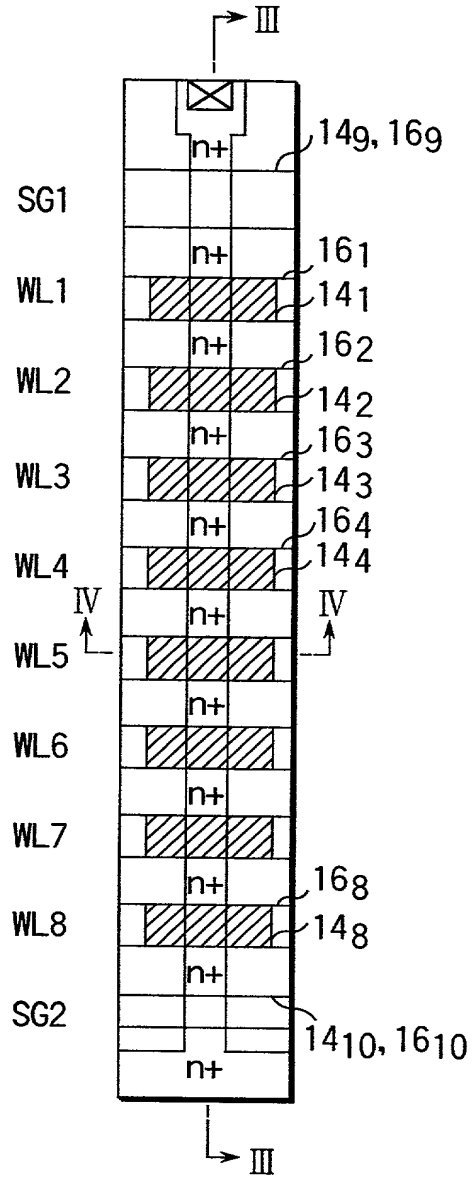


FIG. 2 PRIOR ART

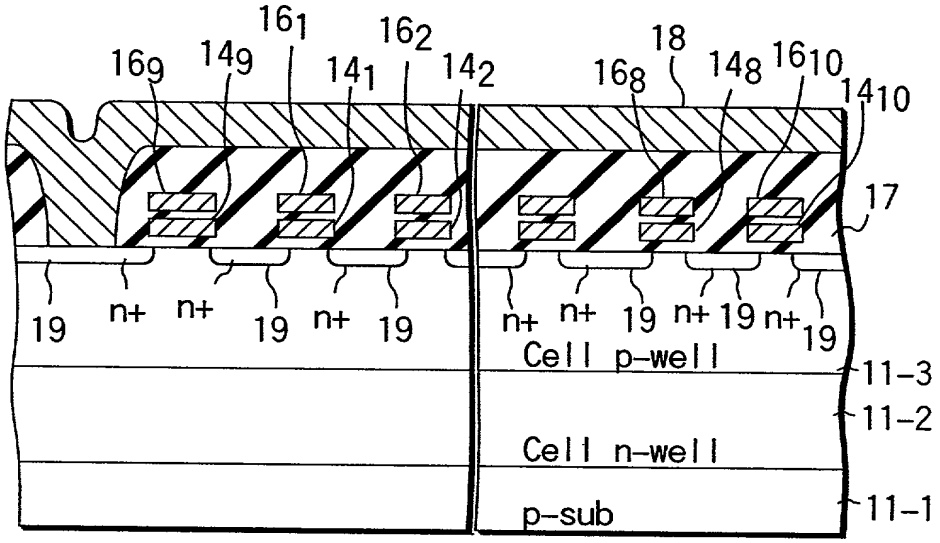


FIG. 3 PRIOR ART

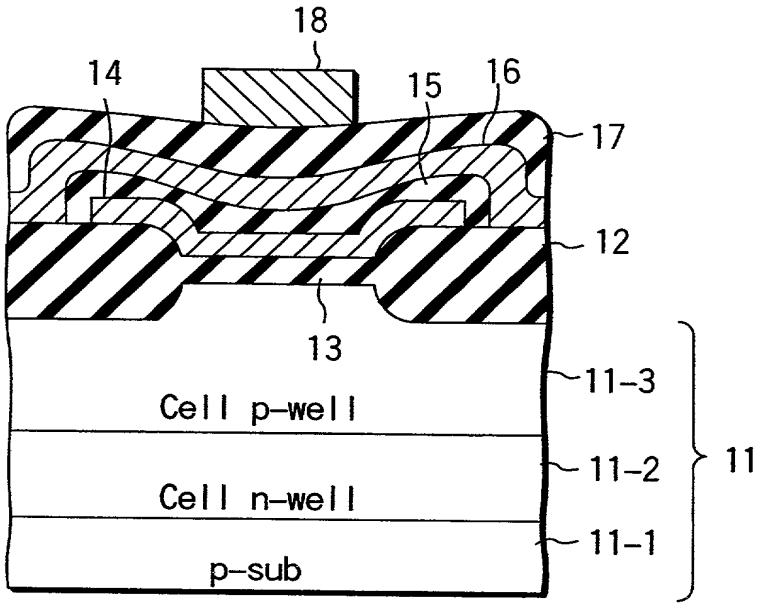


FIG. 4 PRIOR ART

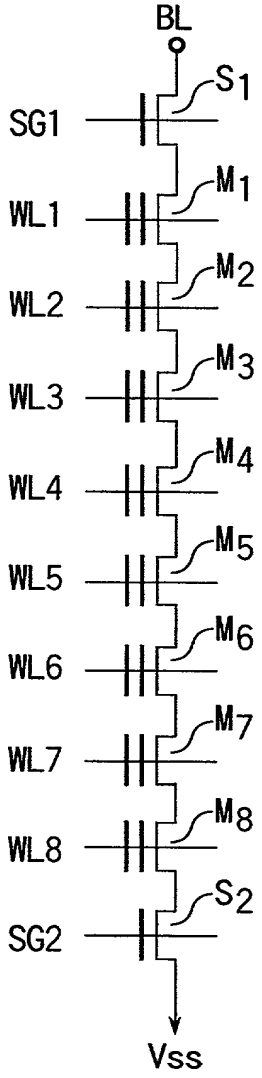


FIG. 5 PRIOR ART

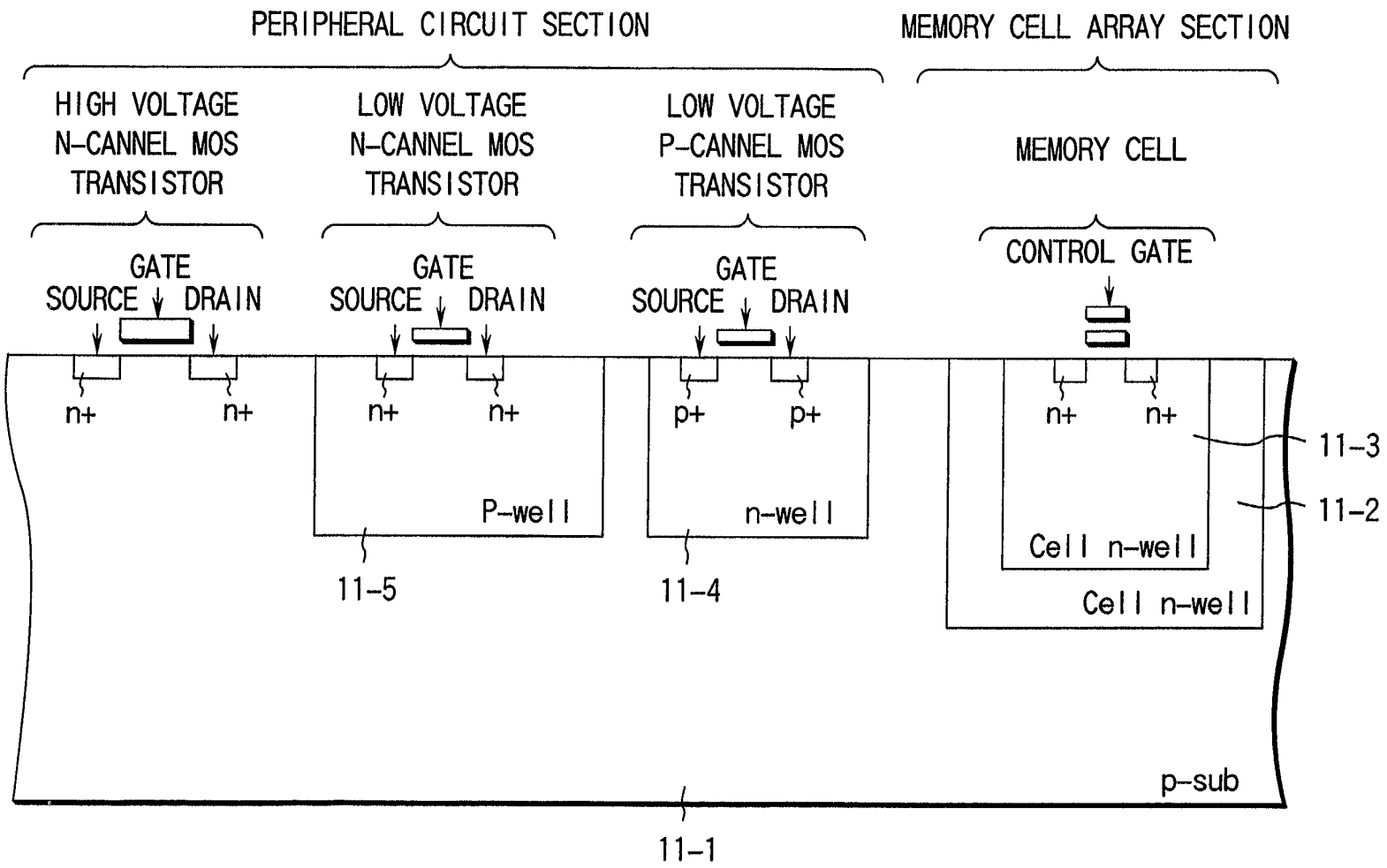


FIG. 6 PRIOR ART

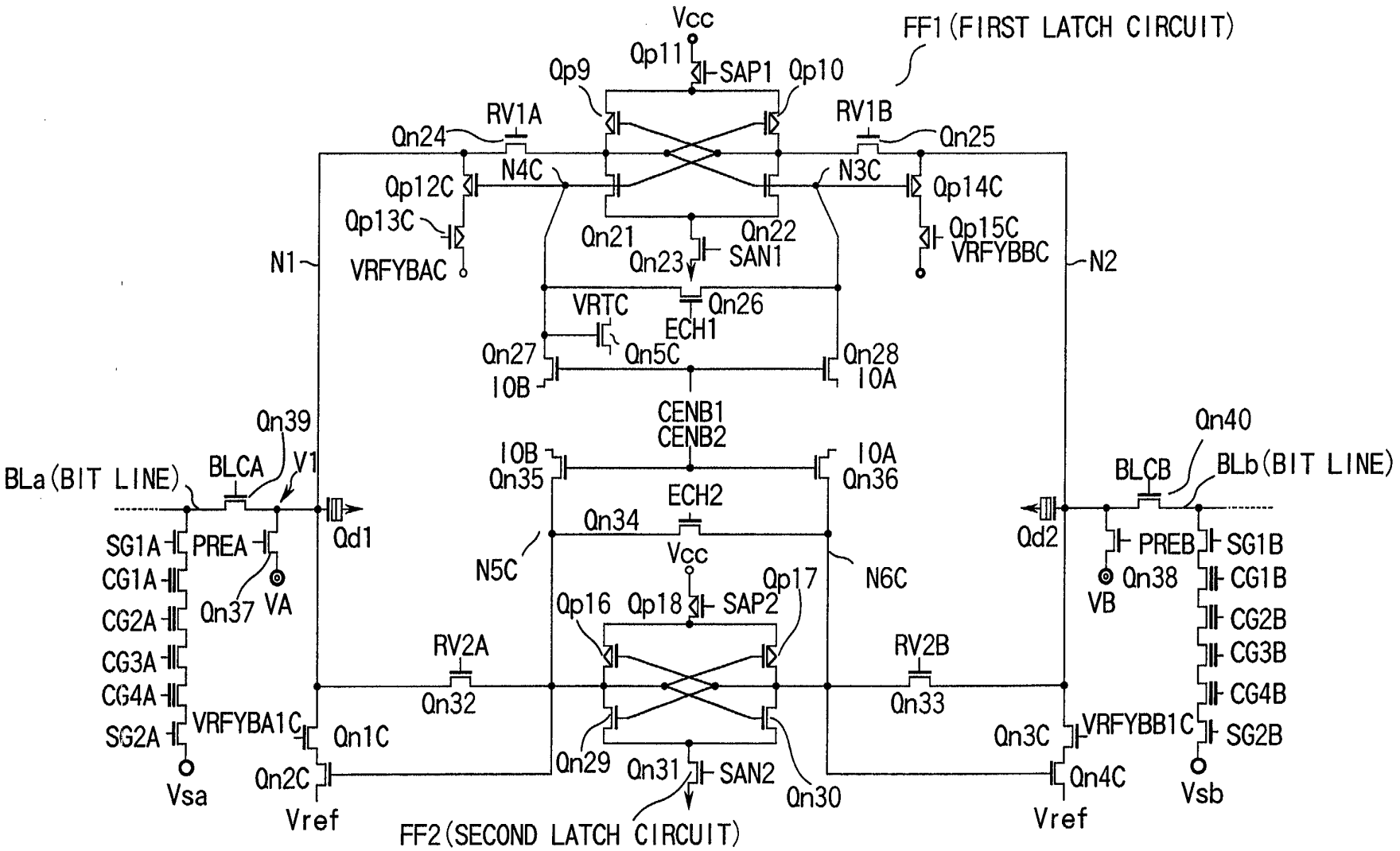


FIG. 7 PRIOR ART

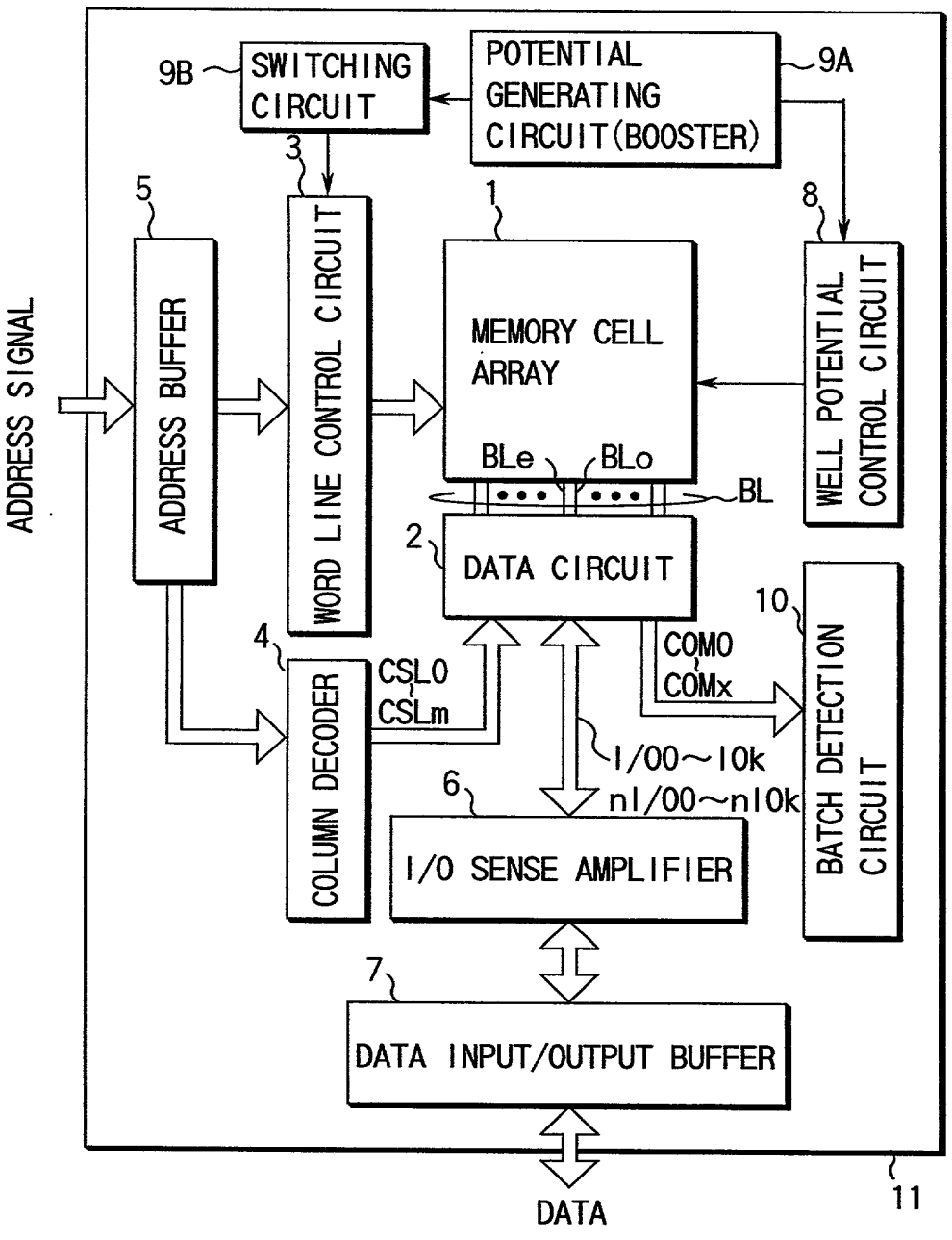
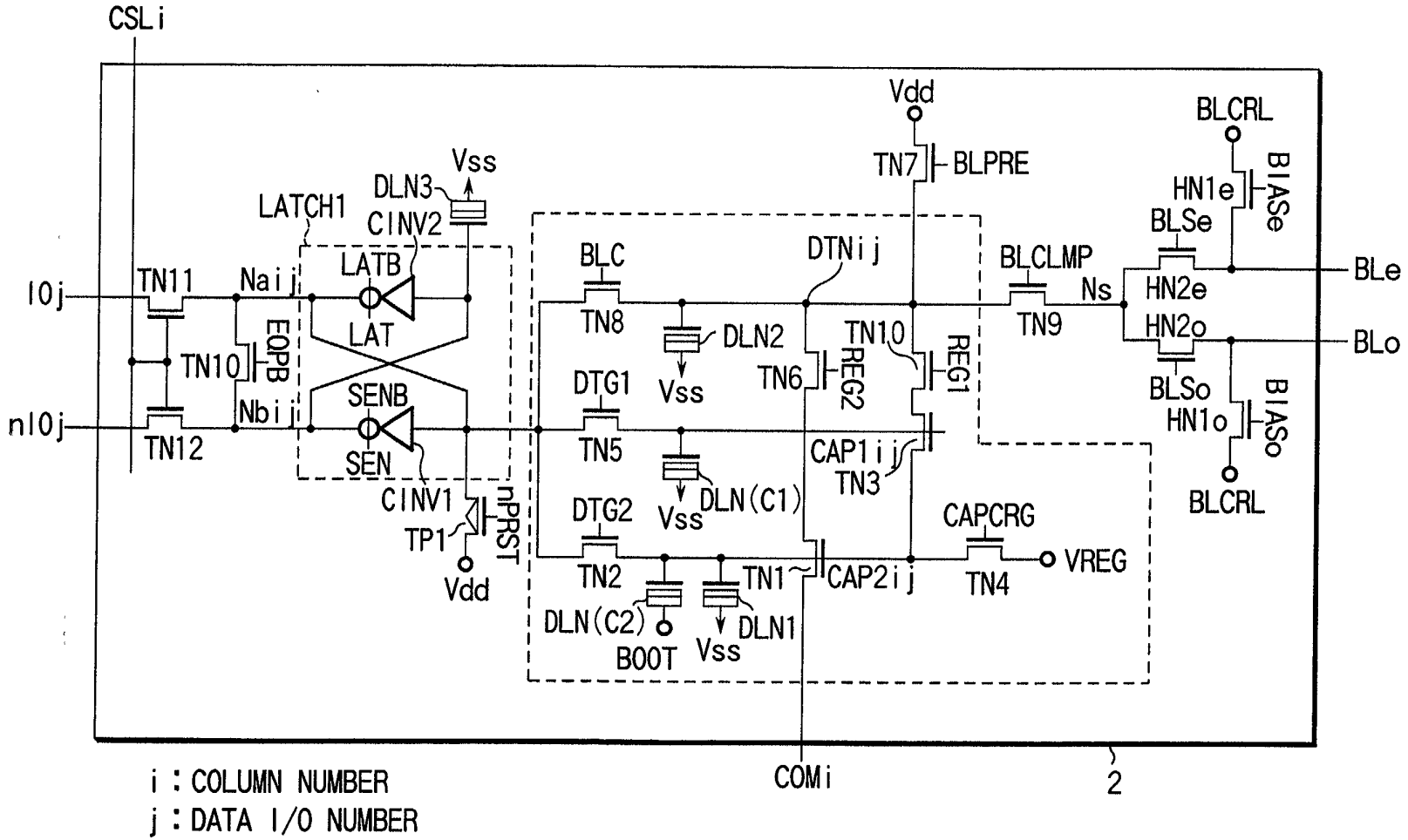


FIG. 8



i : COLUMN NUMBER
j : DATA I/O NUMBER

FIG. 9

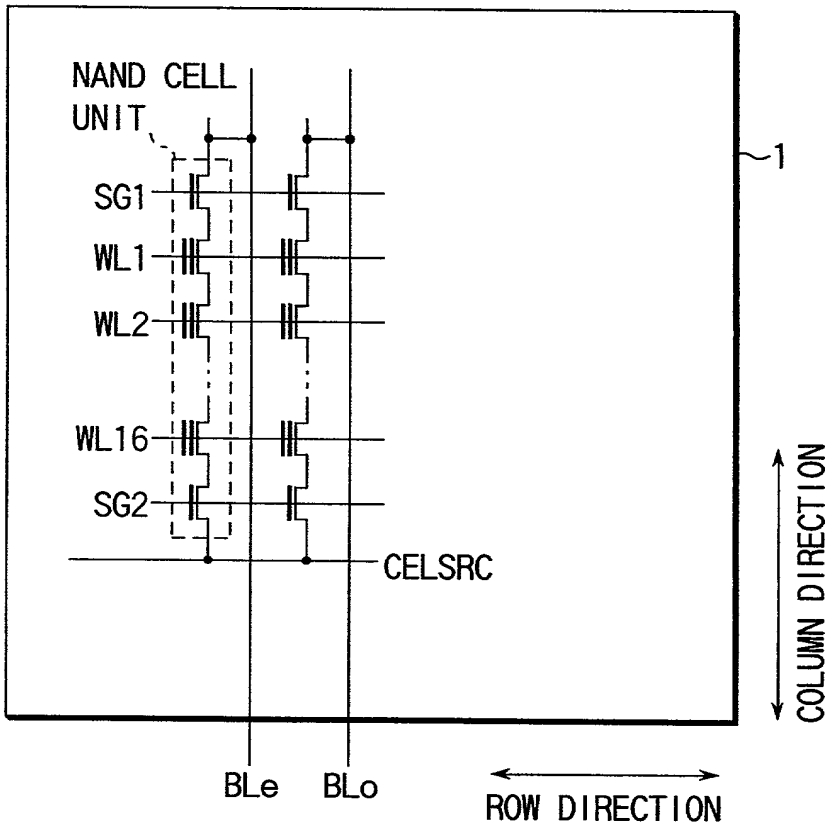


FIG. 10

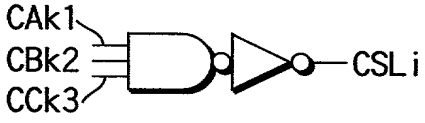


FIG. 11

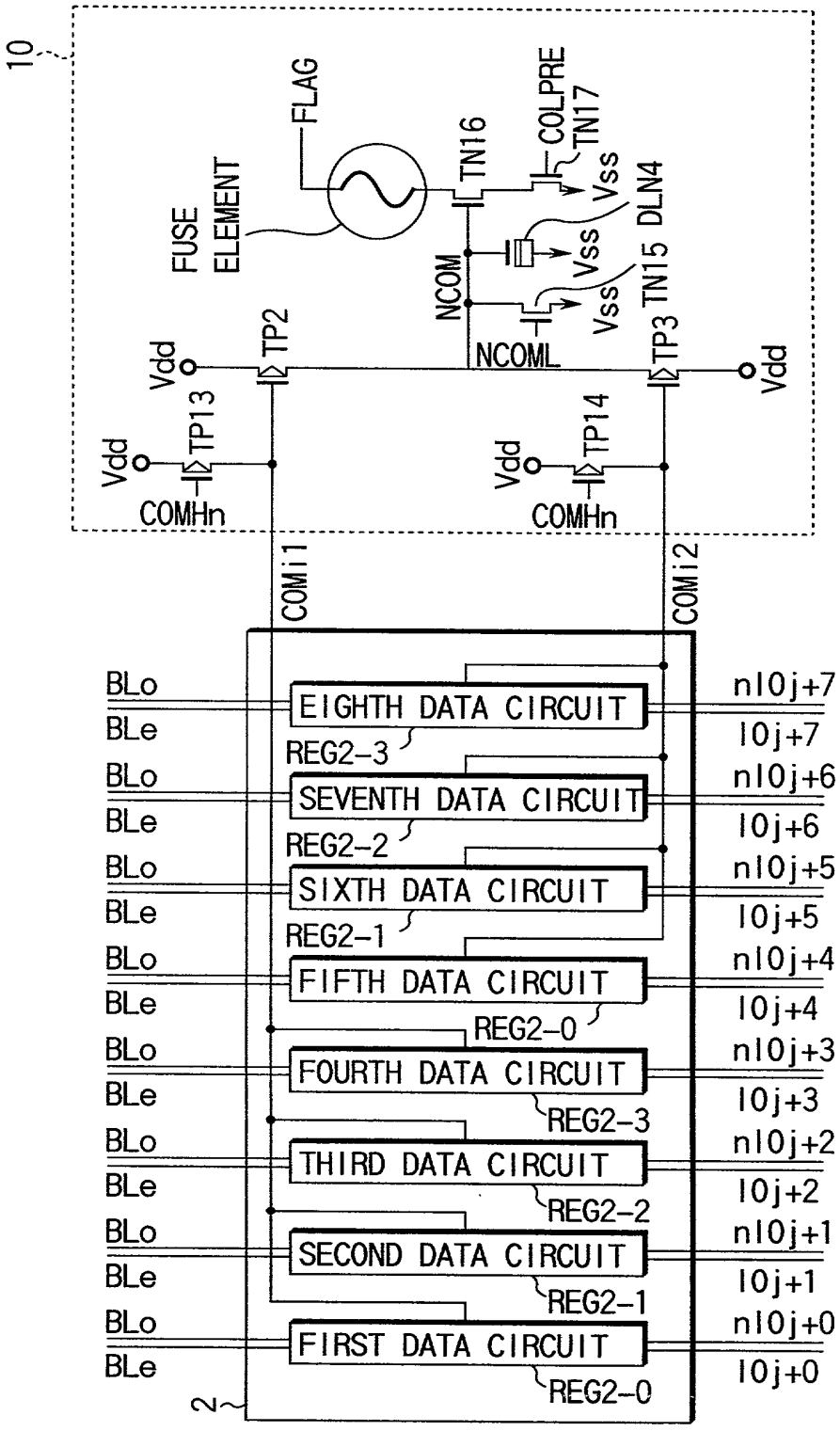
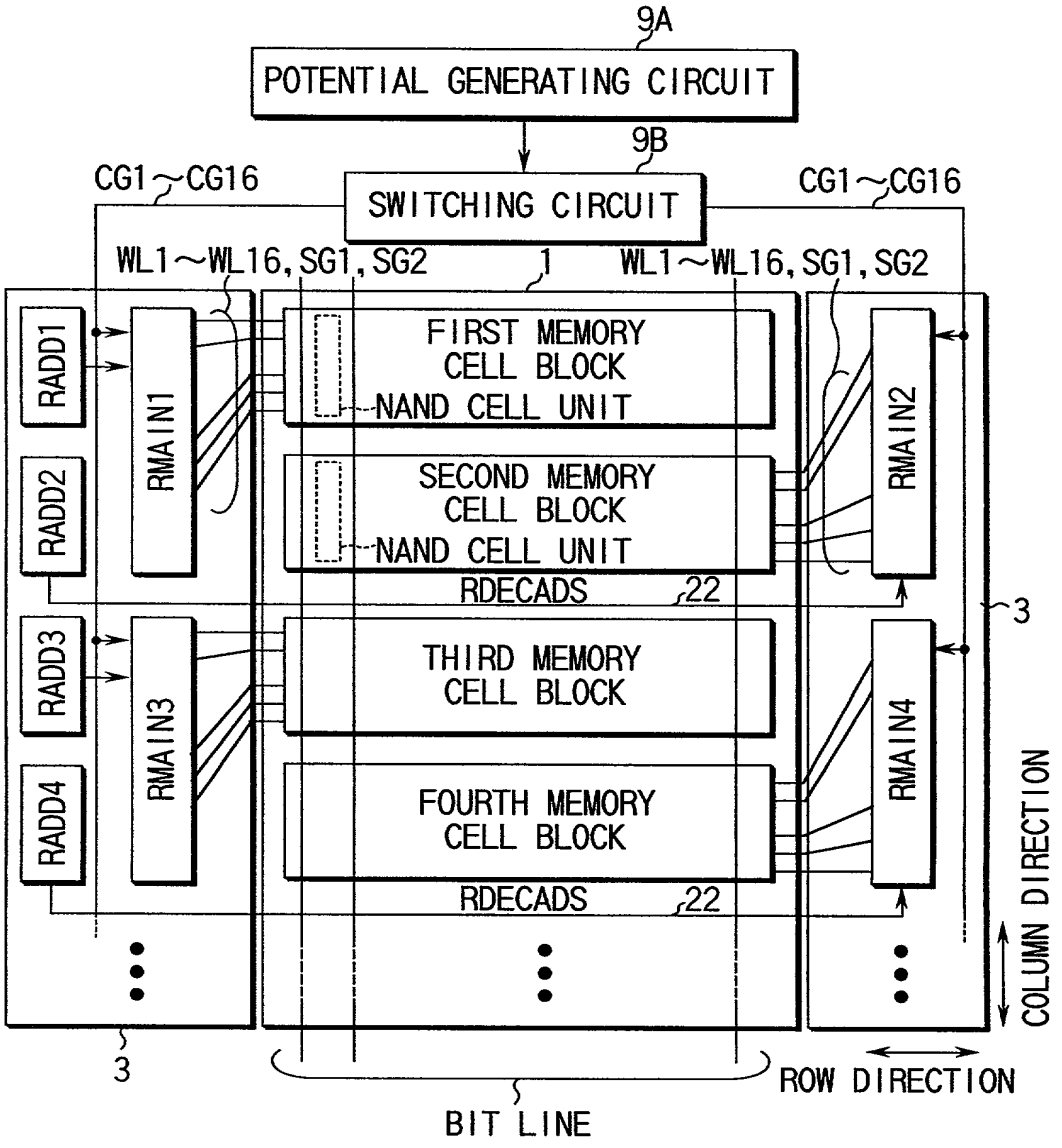


FIG. 12



RMAINi : i-TH WORD LINE DRIVER
RADDi : i-TH ROW ADDRESS DECODER
RDECADSi : WORD LINE DRIVER SELECTING SIGNAL
i=1.2.3.4. • • •

FIG. 13

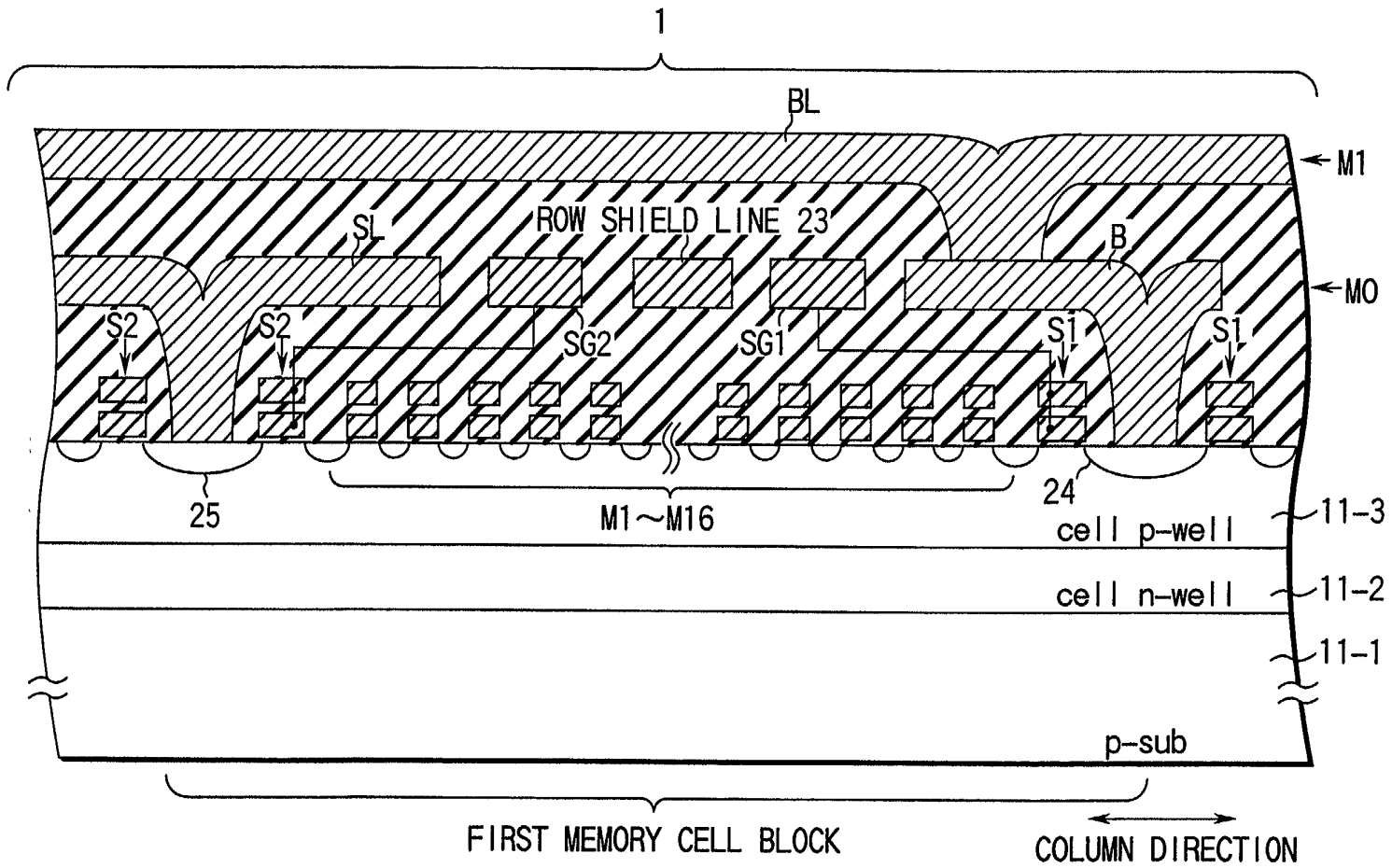


FIG. 14

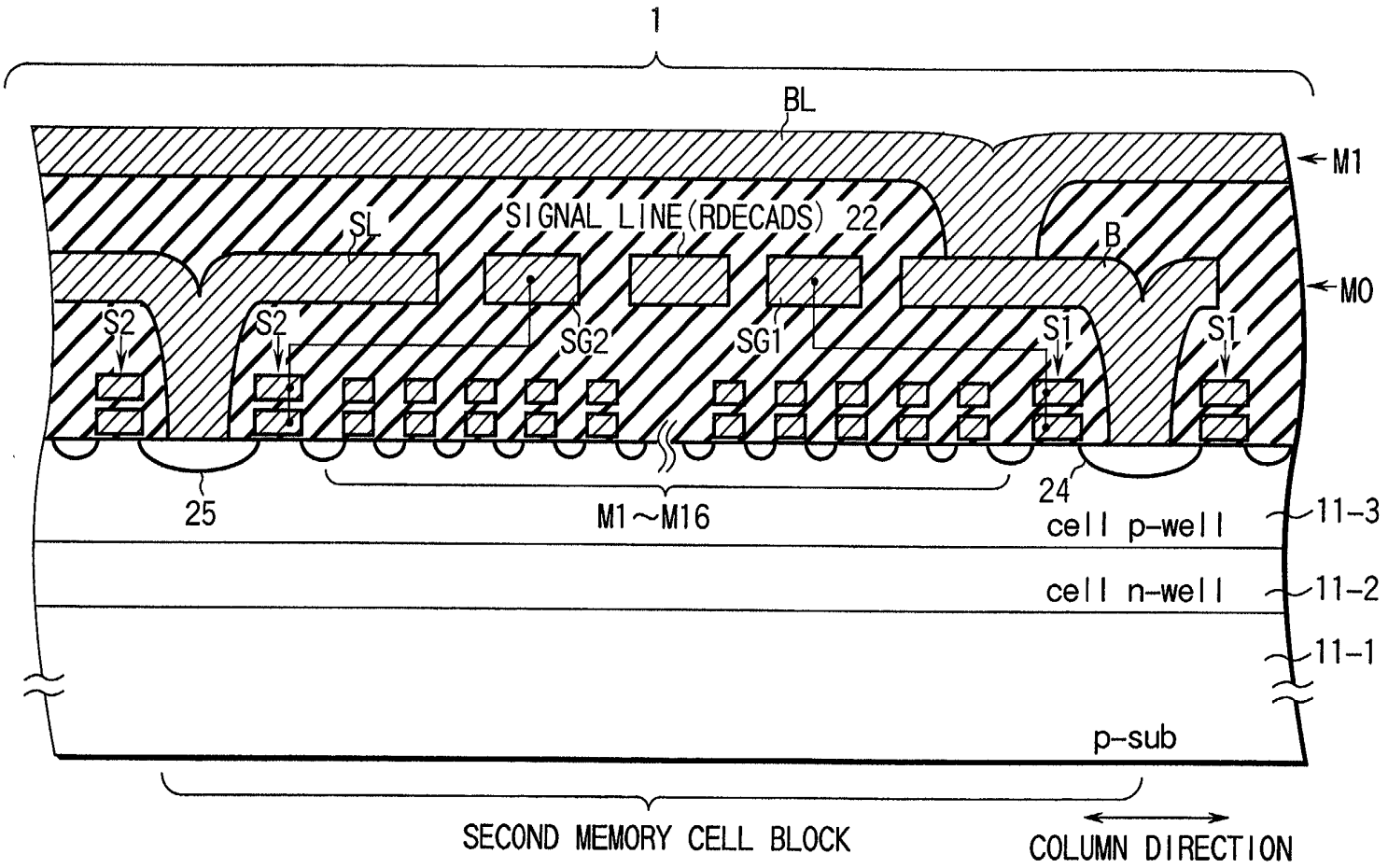

1
BL
M1
SL
SIGNAL LINE(RDECADS) 22
B
M0
S2
S2
SG2
SG1
S1
S1
25
M1~M16
24
cell p-well
11-3
cell n-well
11-2
11-1
p-sub
SECOND MEMORY CELL BLOCK
COLUMN DIRECTION

FIG. 15

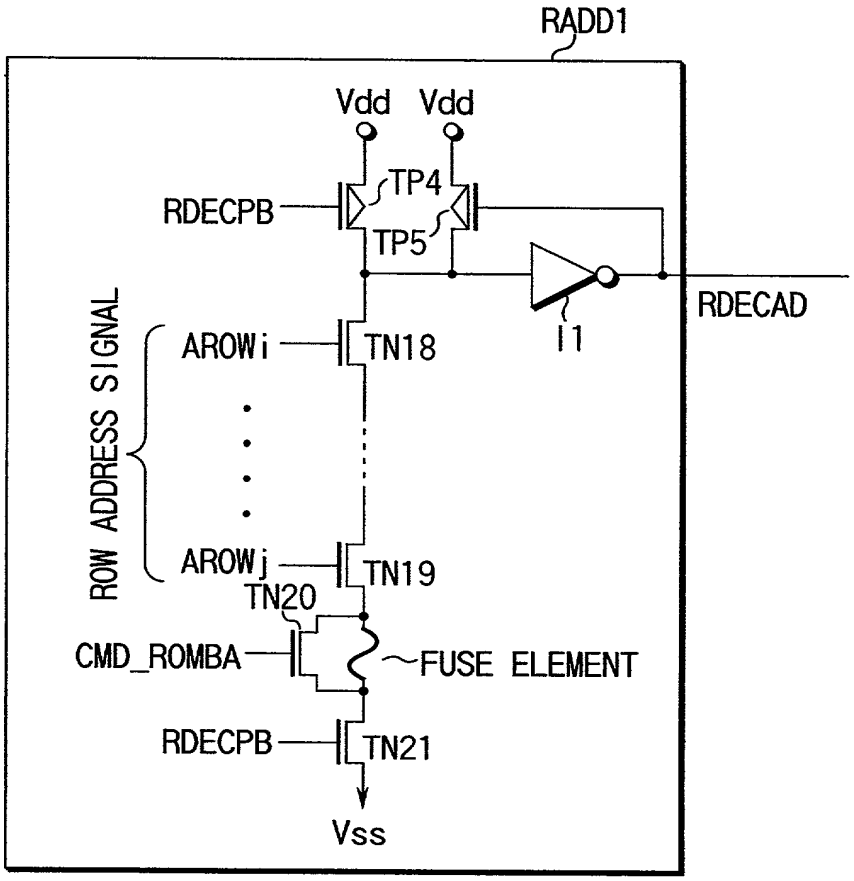


FIG. 16

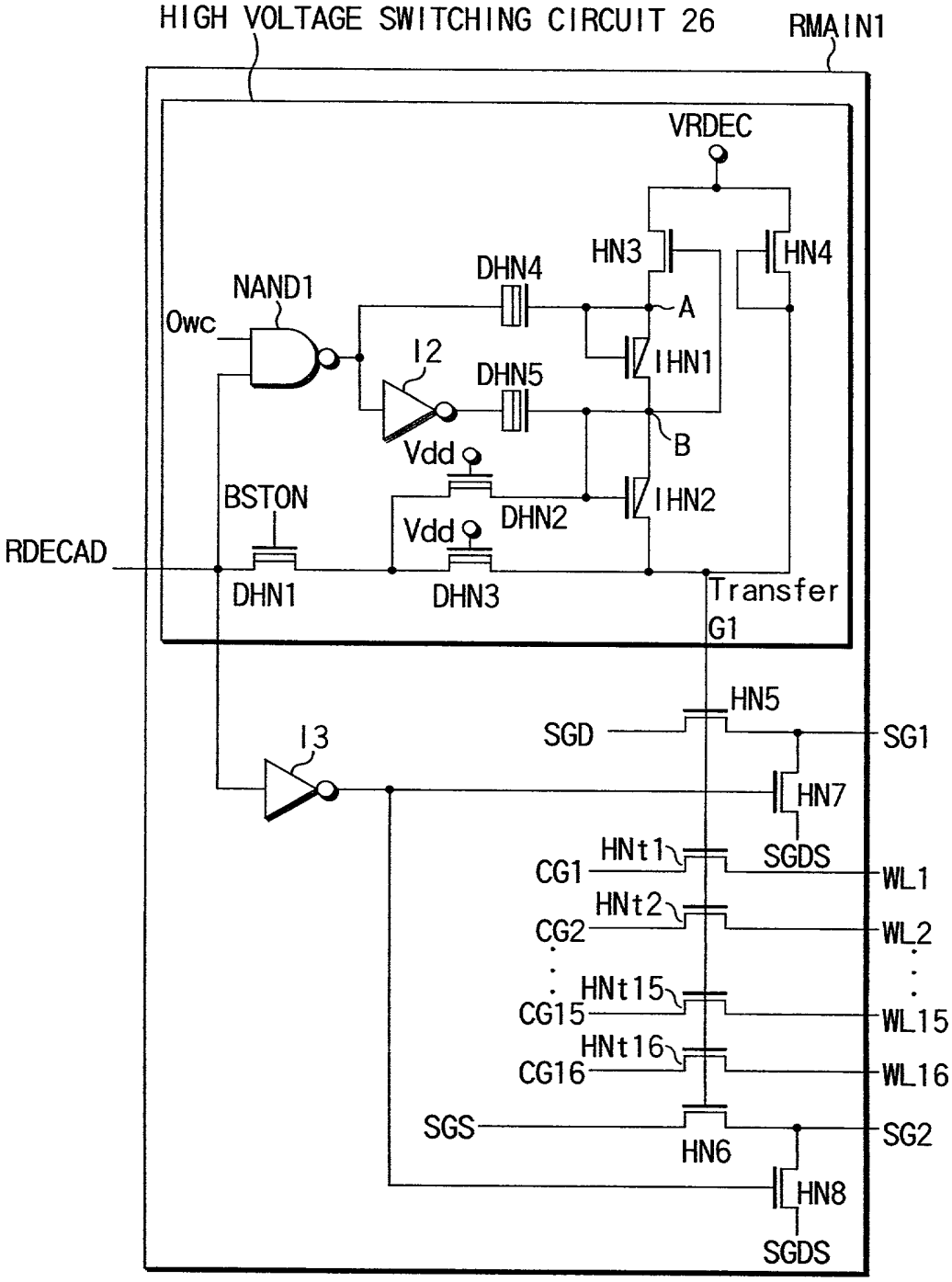


FIG. 17

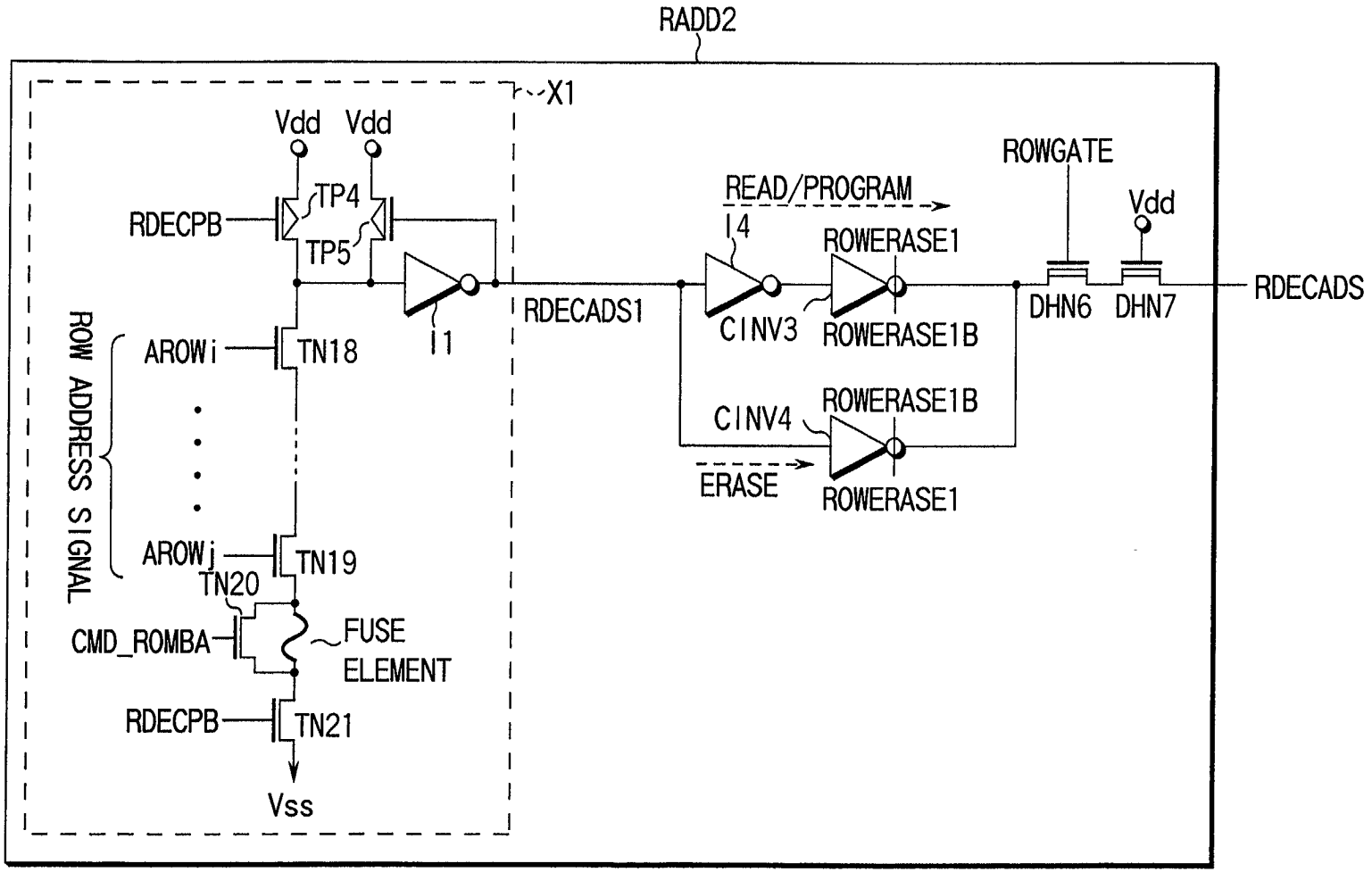

RADD2
X1
Vdd
Vdd
TP4
TP5
RDECPB
ROW ADDRESS SIGNAL
AROWi
TN18
AROWj
TN19
TN20
CMD_ROMBA
FUSE
ELEMENT
RDECPB
TN21
Vss
I1
RDECADS1
READ/PROGRAM
I4
CINV3
ROWERASE1
ROWERASE1B
CINV4
ERASE
ROWERASE1B
ROWERASE1
ROWGATE
Vdd
DHN6
DHN7
RDECADS

FIG. 18

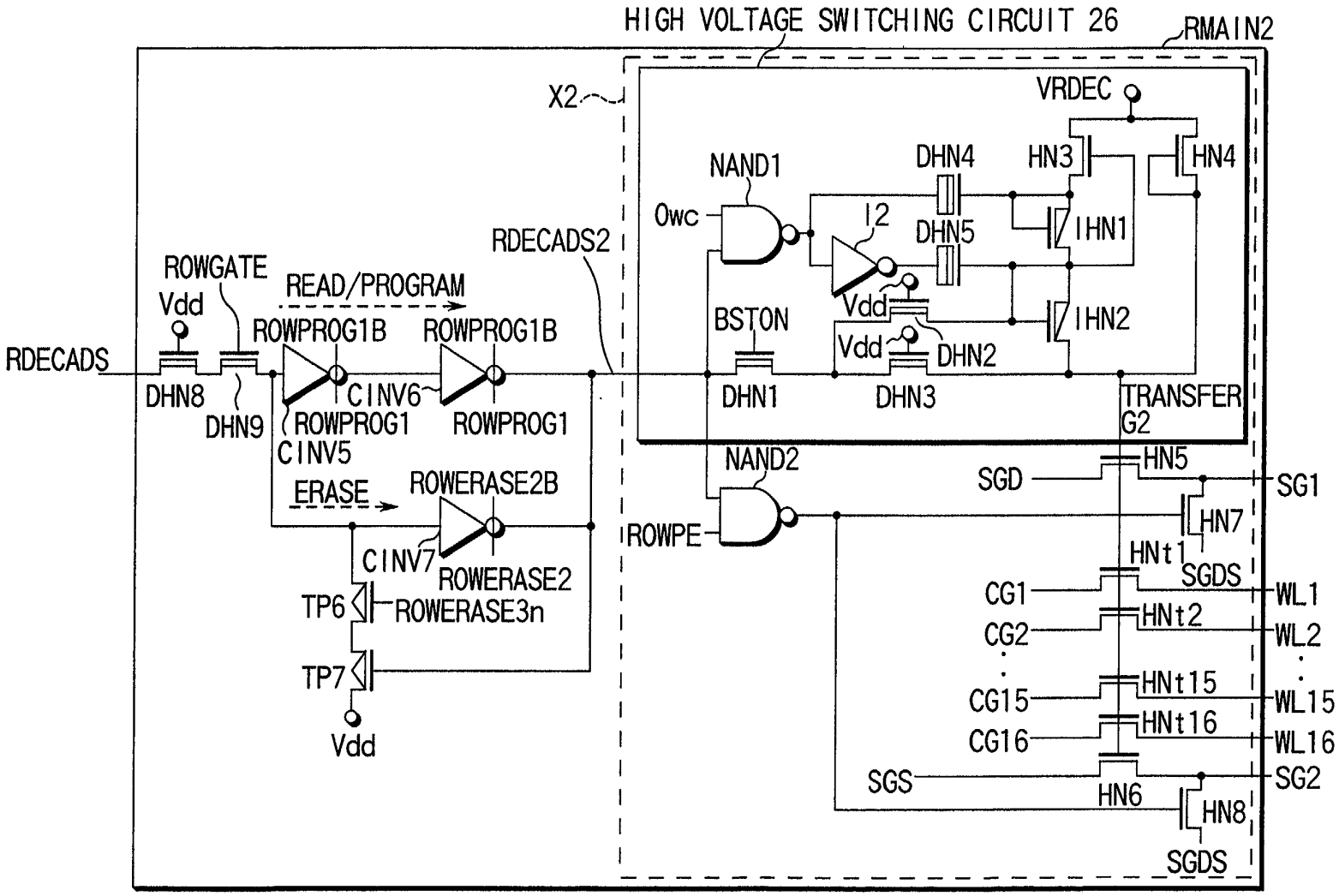

HIGH VOLTAGE SWITCHING CIRCUIT 26
RMAIN2
X2
VRDEC
NAND1
DHN4
HN3
HN4
Owc
I2
DHN5
IHN1
RDECADS2
ROWGATE
READ/PROGRAM
Vdd
ROWPROG1B
ROWPROG1B
BSTON
Vdd
IHN2
RDECADS
Vdd
DHN2
DHN8
DHN9
CINV6
ROWPROG1
ROWPROG1
DHN1
DHN3
TRANSFER G2
CINV5
NAND2
HN5
SGD
SG1
ERASE
ROWERASE2B
HN7
ROWPE
HNt1
SGDS
CINV7
ROWERASE2
CG1
WL1
TP6
ROWERASE3n
HNt2
CG2
WL2
TP7
HNt15
CG15
WL15
HNt16
CG16
WL16
Vdd
SGS
SG2
HN6
HN8
SGDS

FIG. 19

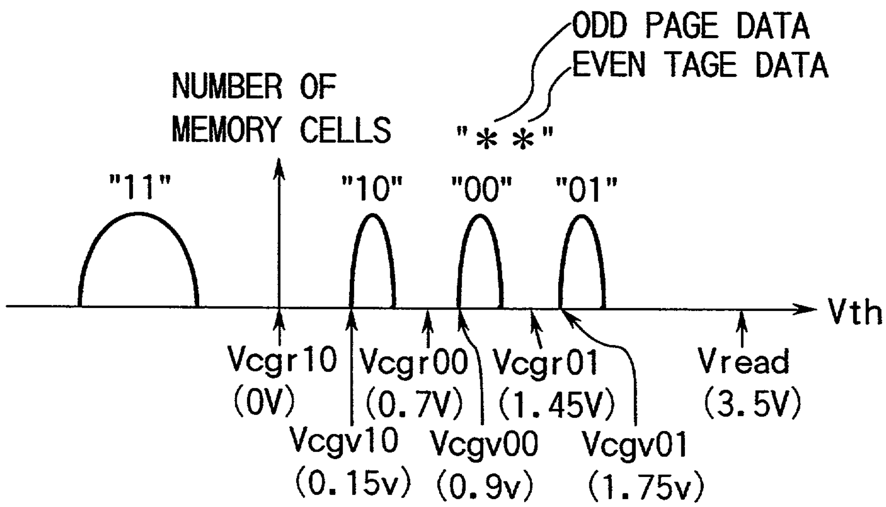


FIG. 20

PROGRAM OF EVEN PAGE DATA

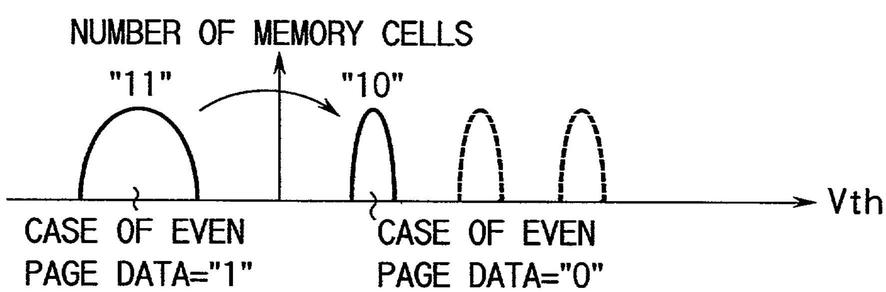


FIG. 21

PROGRAM OF ODD PAGE DATA

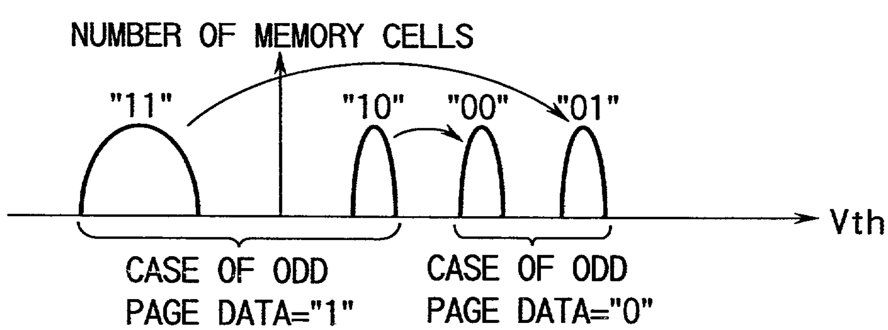


FIG. 22

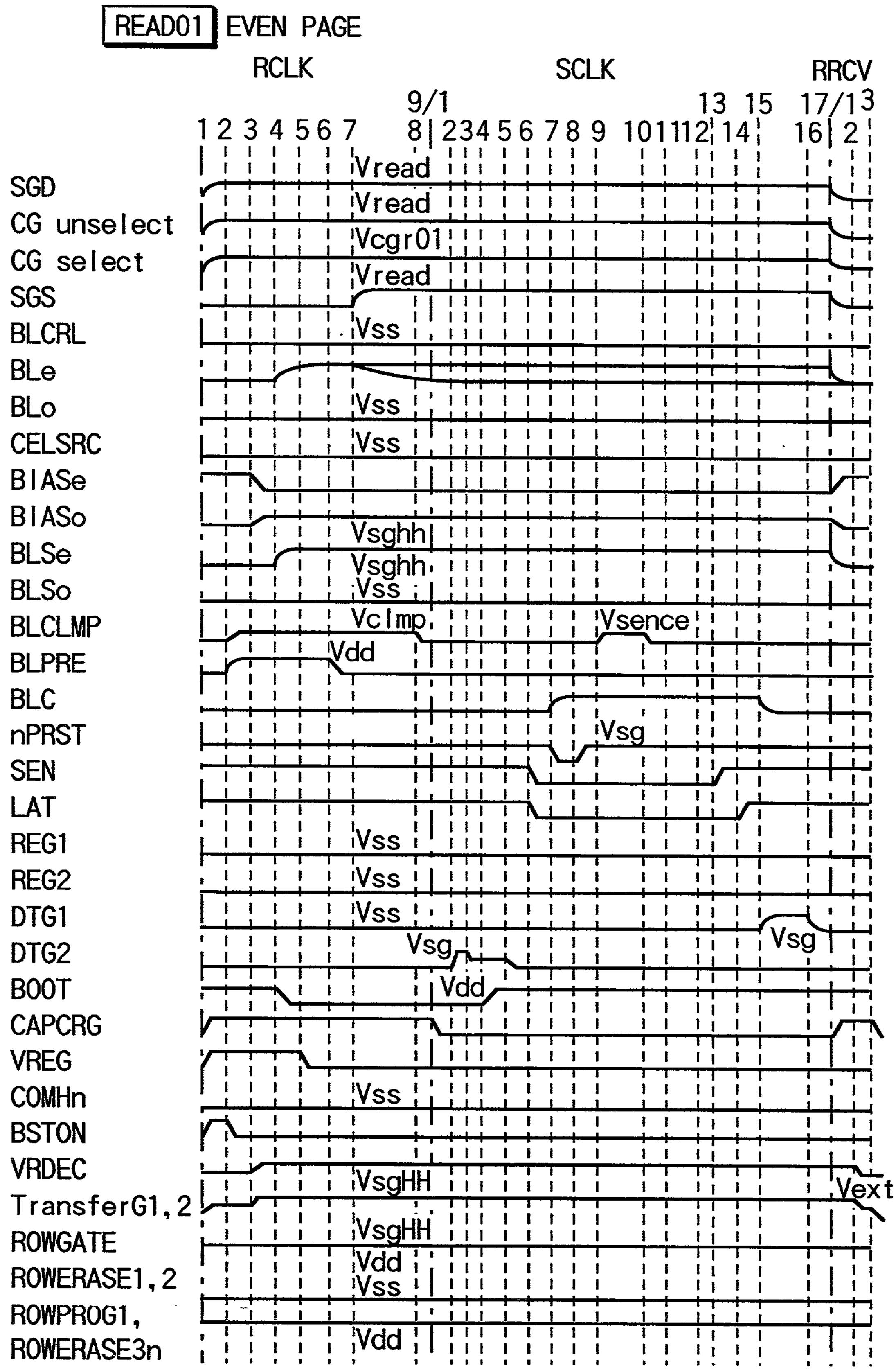

READ01 EVEN PAGE
RCLK
SCLK
RRCV
1 2 3 4 5 6 7 8 9/1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17/1 2 3
SGD
CG unselect
CG select
SGS
BLCRL
BLe
BLo
CELSRC
BIASe
BIASo
BLSe
BLSo
BLCLMP
BLPRE
BLC
nPRST
SEN
LAT
REG1
REG2
DTG1
DTG2
BOOT
CAPCRG
VREG
COMHn
BSTON
VRDEC
TransferG1,2
ROWGATE
ROWERASE1,2
ROWPROG1,
ROWERASE3n
Vread
Vread
Vcgr01
Vread
Vss
Vss
Vss
Vsghh
Vsghh
Vss
Vclmp
Vsence
Vdd
Vsg
Vss
Vss
Vss
Vsg
Vsg
Vdd
Vss
VsgHH
Vext
VsgHH
Vdd
Vss
Vdd

FIG. 23

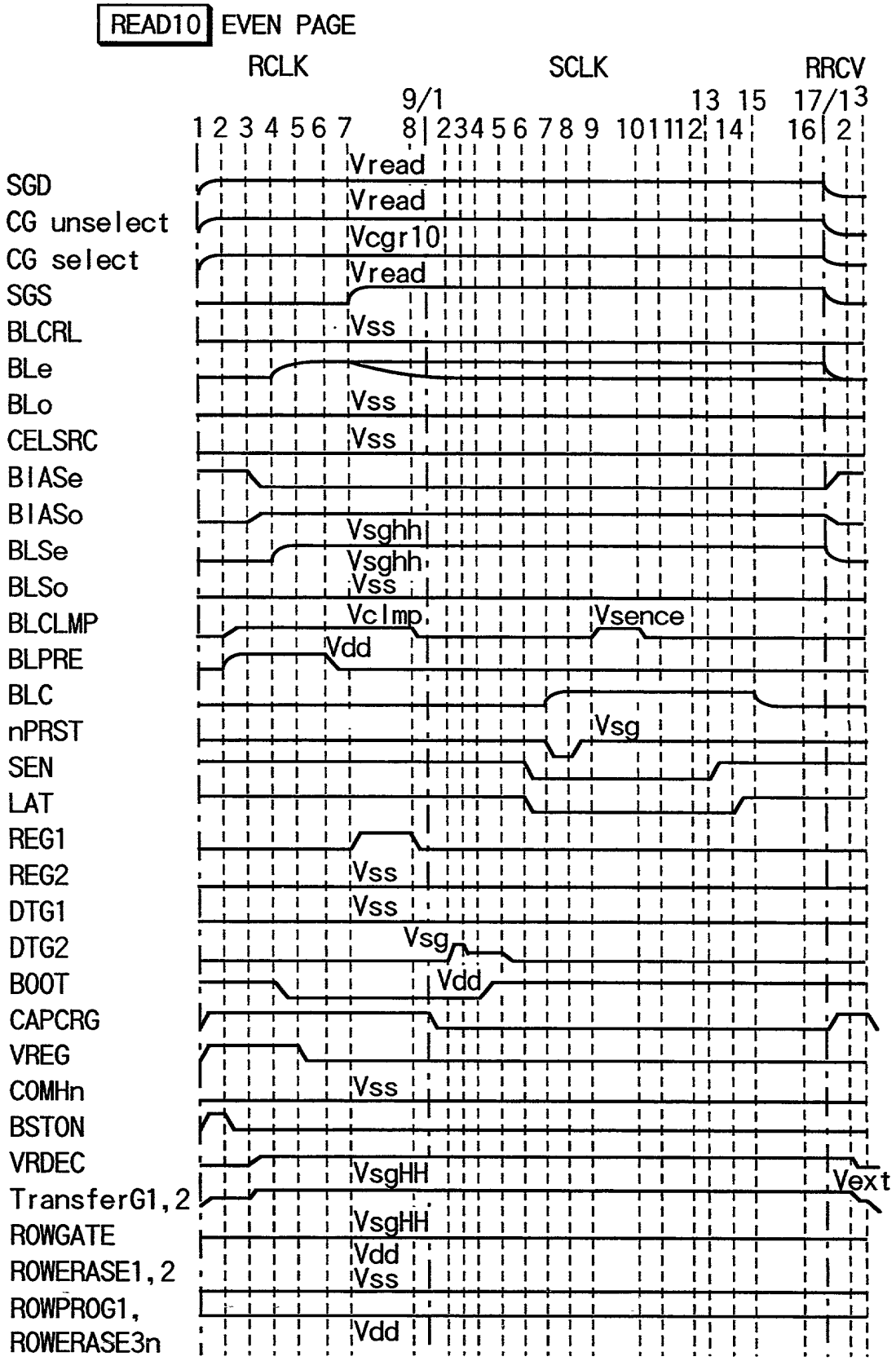

READ10 EVEN PAGE
RCLK
SCLK
RRCV
9/1
13 15
17/13
1 2 3 4 5 6 7 8 2 3 4 5 6 7 8 9 10 11 12 14 16 2
SGD
CG unselect
CG select
SGS
BLCRL
BLe
BLo
CELSRC
BIASe
BIASo
BLSe
BLSo
BLCLMP
BLPRE
BLC
nPRST
SEN
LAT
REG1
REG2
DTG1
DTG2
BOOT
CAPCRG
VREG
COMHn
BSTON
VRDEC
TransferG1,2
ROWGATE
ROWERASE1,2
ROWPROG1,
ROWERASE3n
Vread
Vcgr10
Vss
Vsghh
Vclmp
Vsence
Vdd
Vsg
VsgHH
Vext

FIG. 24

READ OF EVEN PAGE DATA

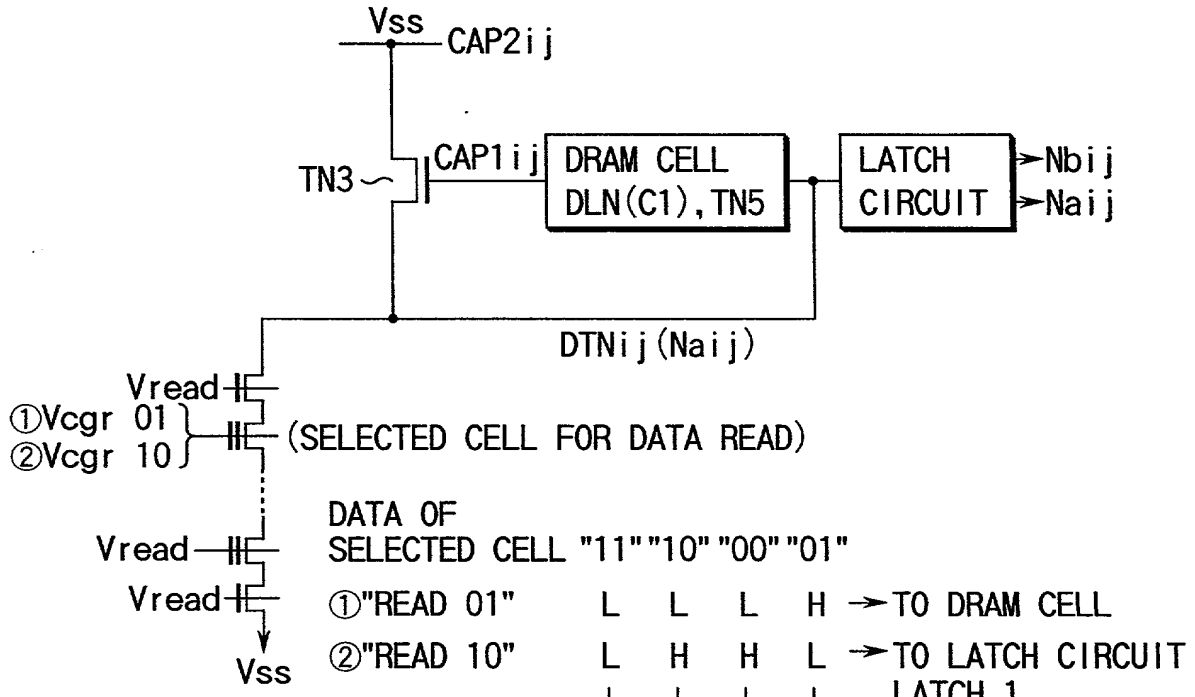


FIG. 25

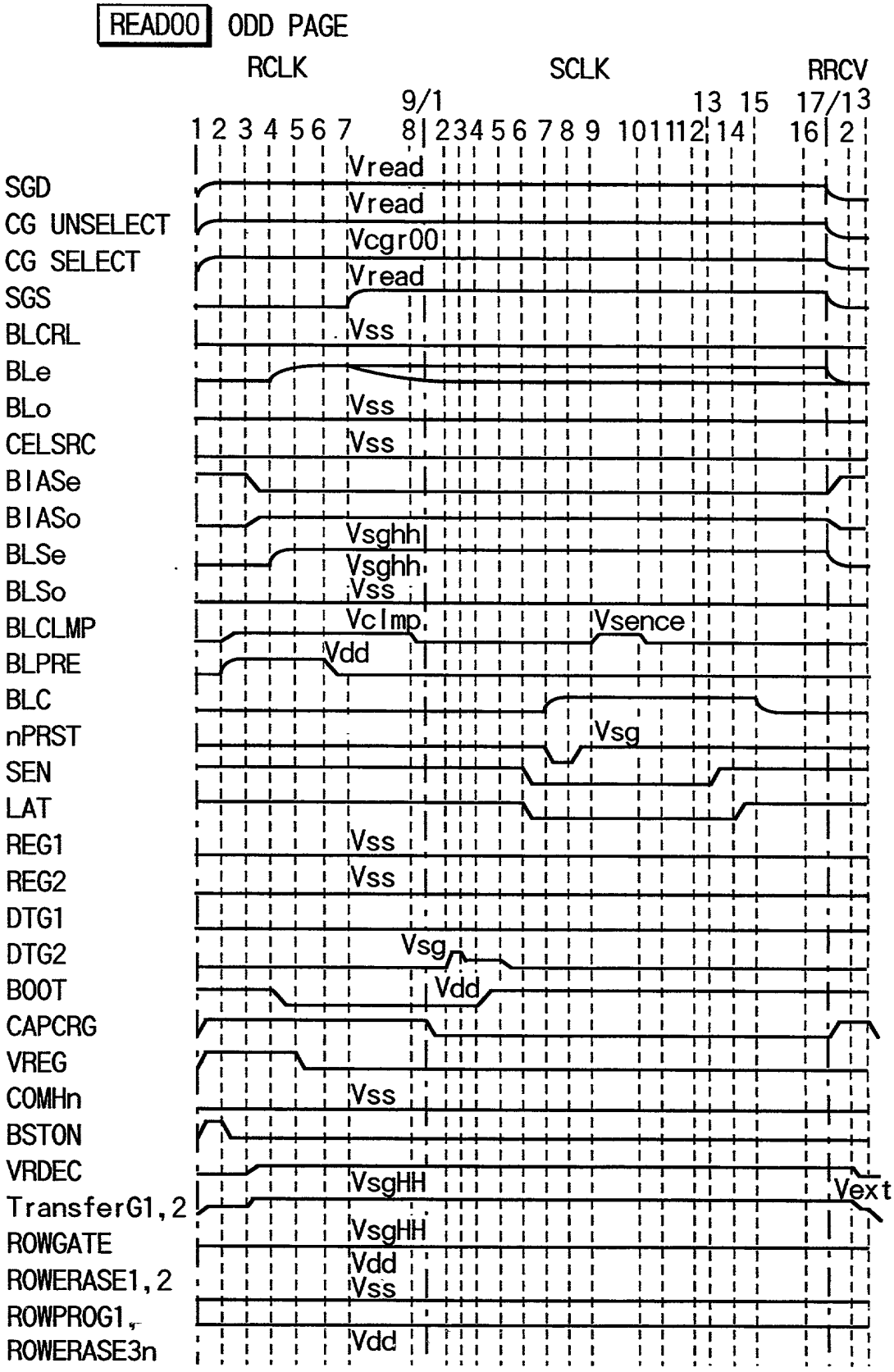

READ00
ODD PAGE
RCLK
SCLK
RRCV
9/1
1 2 3 4 5 6 7 8 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17/1 2 3
SGD
CG UNSELECT
CG SELECT
SGS
BLCRL
BLe
BLo
CELSRC
BIASe
BIASo
BLSe
BLSo
BLCLMP
BLPRE
BLC
nPRST
SEN
LAT
REG1
REG2
DTG1
DTG2
BOOT
CAPCRG
VREG
COMHn
BSTON
VRDEC
TransferG1, 2
ROWGATE
ROWERASE1, 2
ROWPROG1,
ROWERASE3n
Vread
Vread
Vcgr00
Vread
Vss
Vss
Vss
Vsghh
Vsghh
Vss
VcImp
Vsence
Vdd
Vsg
Vss
Vss
Vsg
Vdd
Vss
VsgHH
Vext
VsgHH
Vdd
Vss
Vdd

FIG. 26

READ OF ODD PAGE DATA

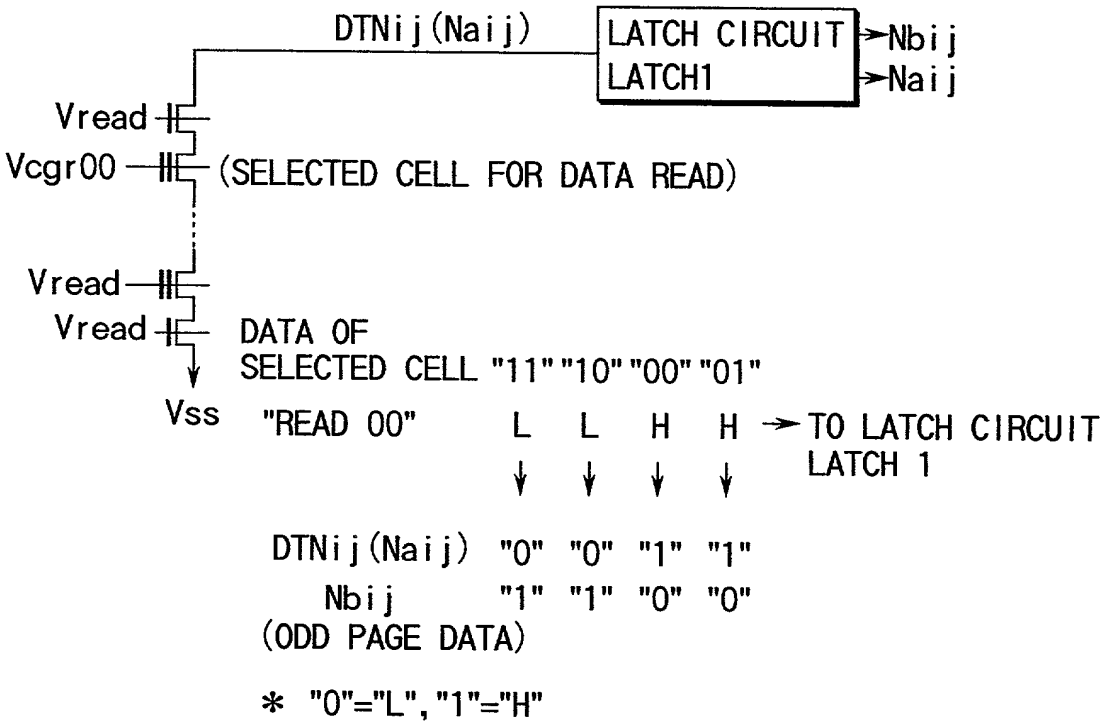


FIG. 27

PROGRAM OPERATION OF EVEN PAGE DATA

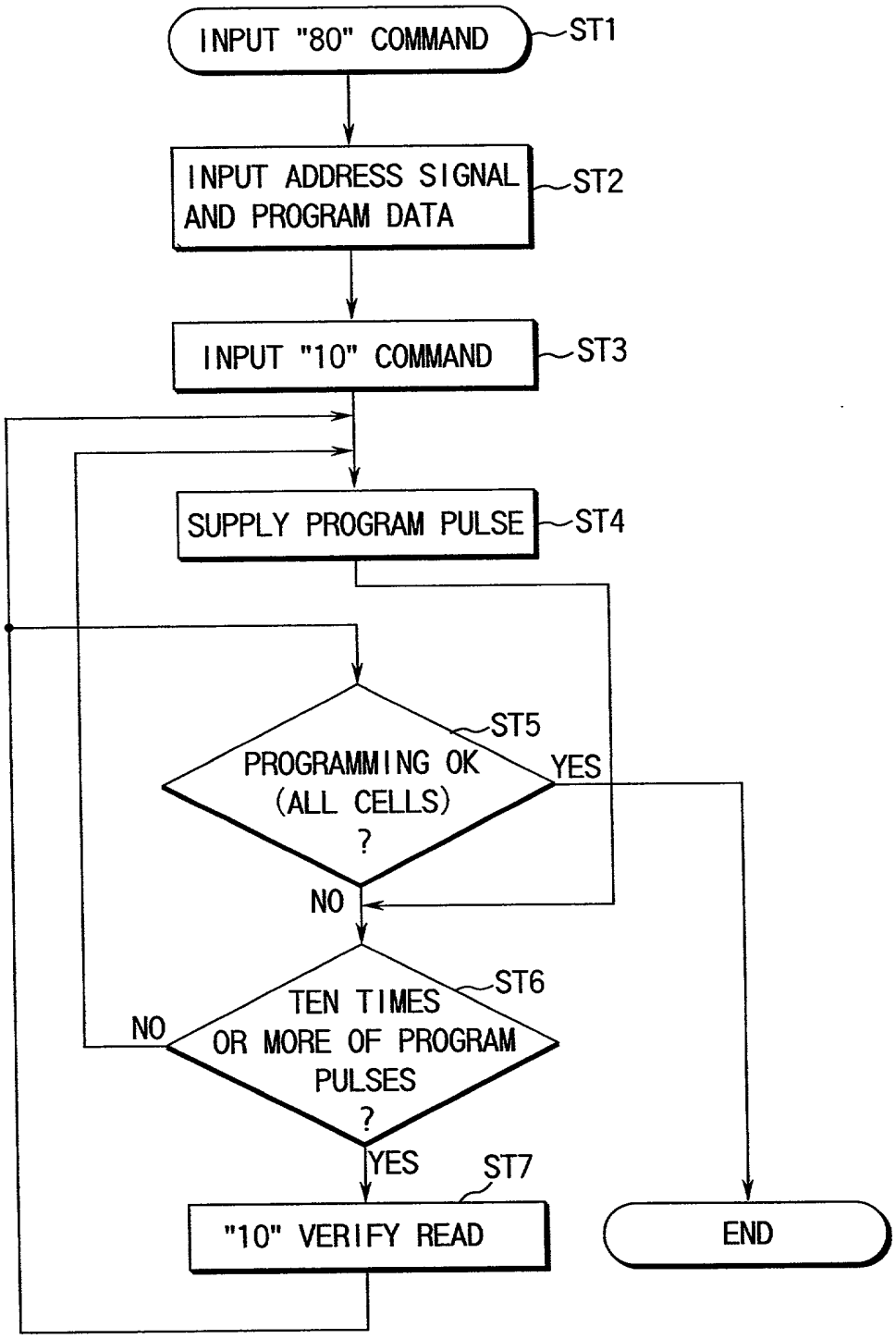


FIG. 28

PROGRAM WHEN LSB,WLs NEIGHBORING SELECTED WL SET Vss
PROGRAM COMPLETION DETECTION IS OPERATED TOO
IN PERIOD CCLK1～10

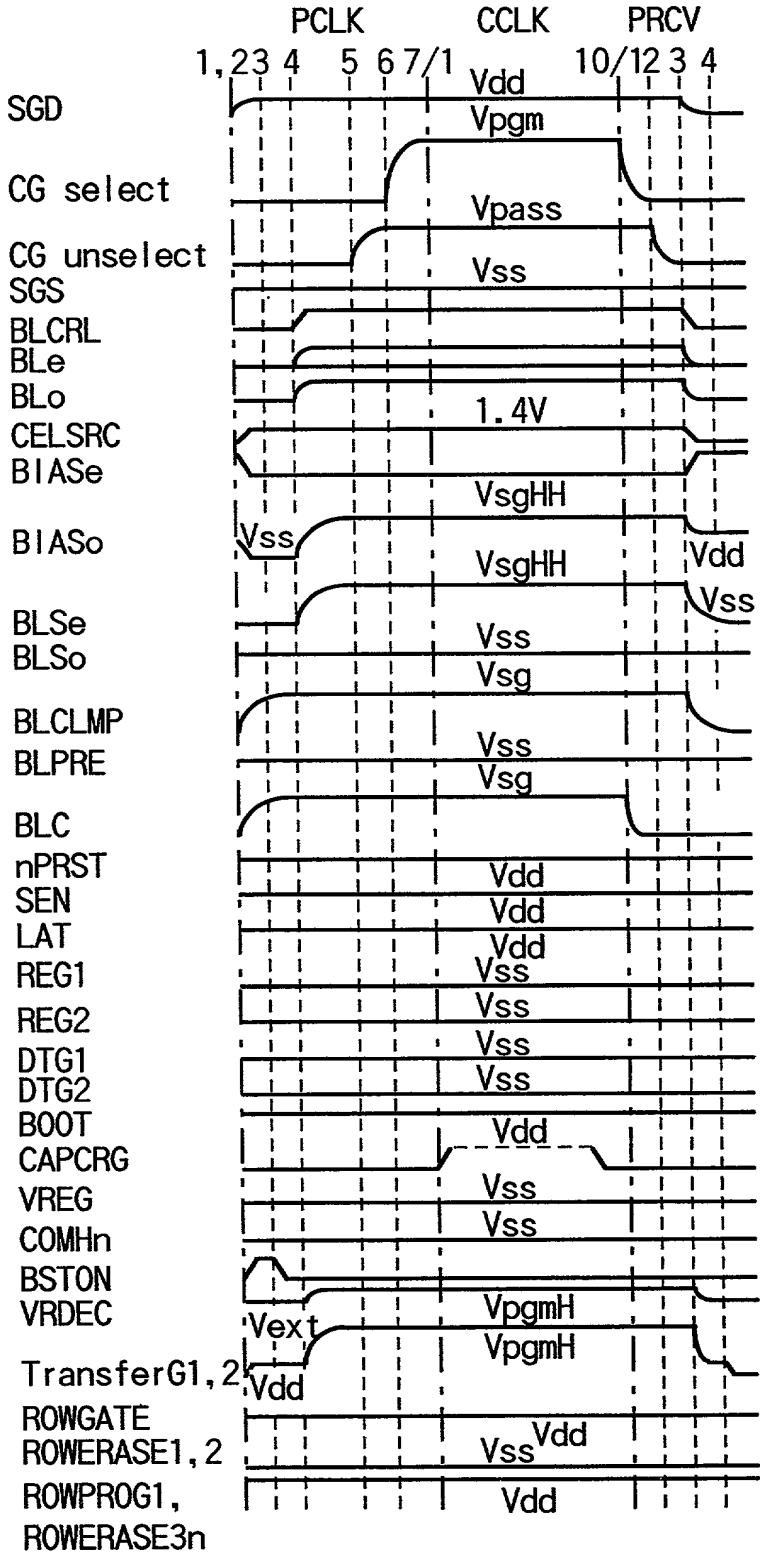


FIG. 29

PROGRAM OF EVEN PAGE DATA (SUPPLY PROGRAM PULSE)

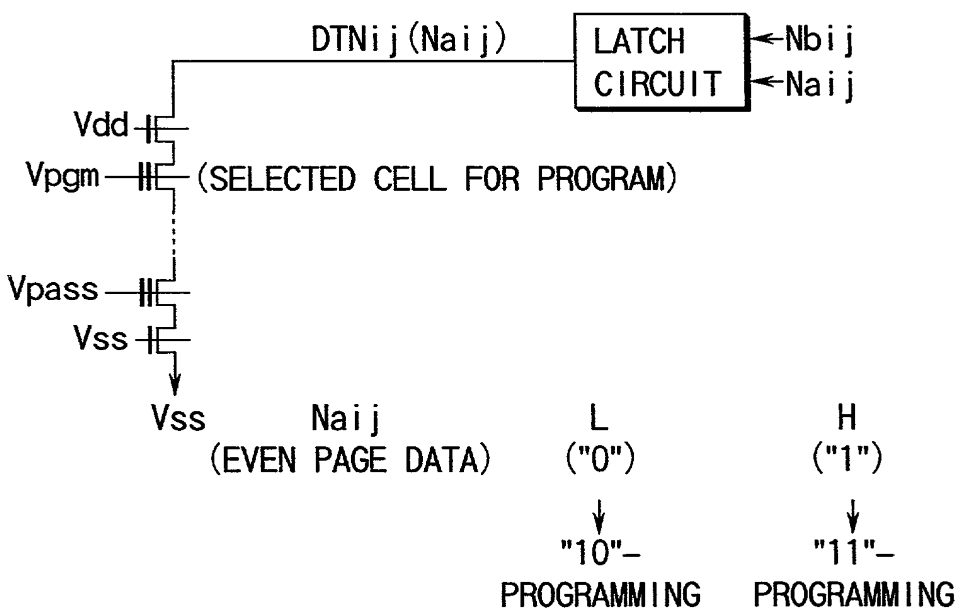


FIG. 30

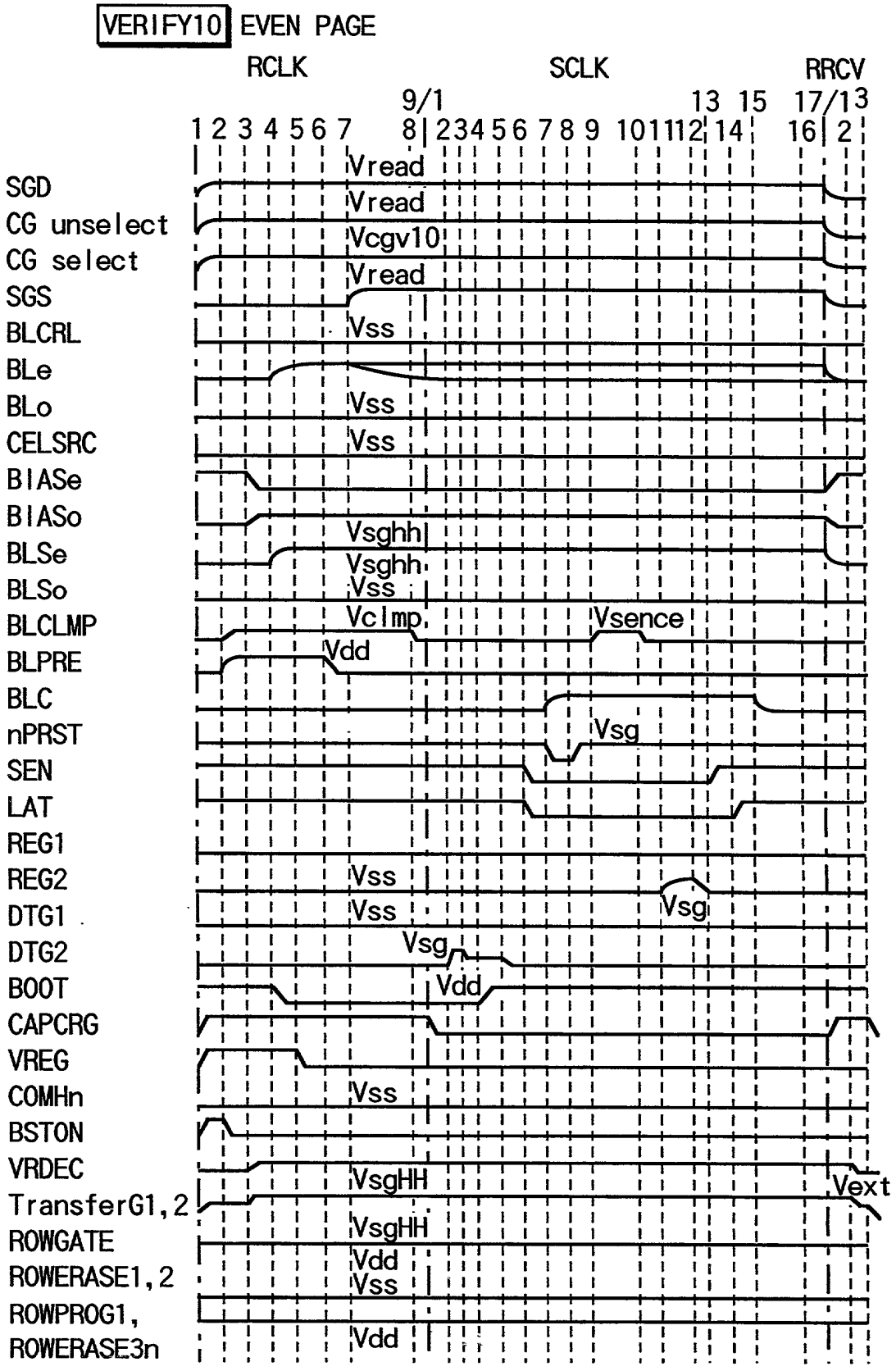
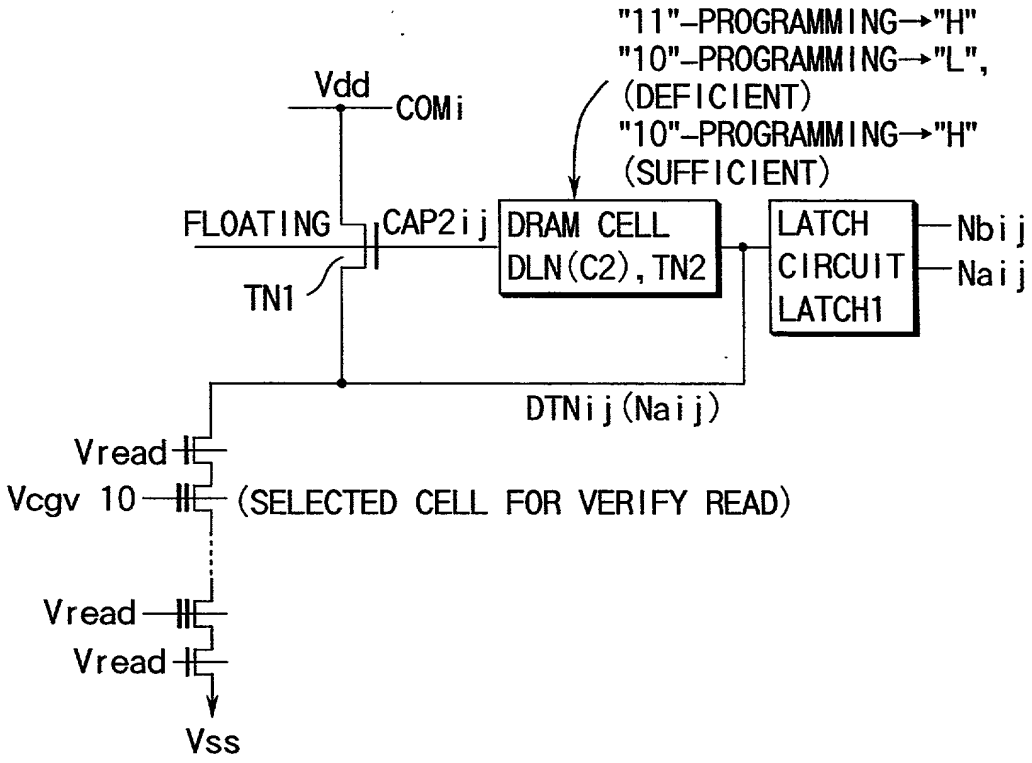

VERIFY10 EVEN PAGE
RCLK
SCLK
RRCV
9/1
13 15
17/13
1 2 3 4 5 6 7 8 2 3 4 5 6 7 8 9 10 11 12 13 14 16 2
SGD
CG unselect
CG select
SGS
BLCRL
BLe
BLo
CELSRC
BIASe
BIASo
BLSe
BLSo
BLCLMP
BLPRE
BLC
nPRST
SEN
LAT
REG1
REG2
DTG1
DTG2
BOOT
CAPCRG
VREG
COMHn
BSTON
VRDEC
TransferG1,2
ROWGATE
ROWERASE1,2
ROWPROG1,
ROWERASE3n
Vread
Vcgv10
Vss
Vsghh
Vclmp
Vsence
Vdd
Vsg
VsgHH
Vext

FIG. 31

PROGRAM OF EVEN PAGE DATA ("10" VERIFY READ)



STATE OF SELECTED CELL	"11"-PROGRAMMING "11"	"10"-PROGRAMMING "10"DEFICIENT	"10"SUFFICIENT
BIT LINE	L	L	H
DTNij(Naij)	H	L	H → TO LATCH CIRCUIT LATCH1

FIG. 32

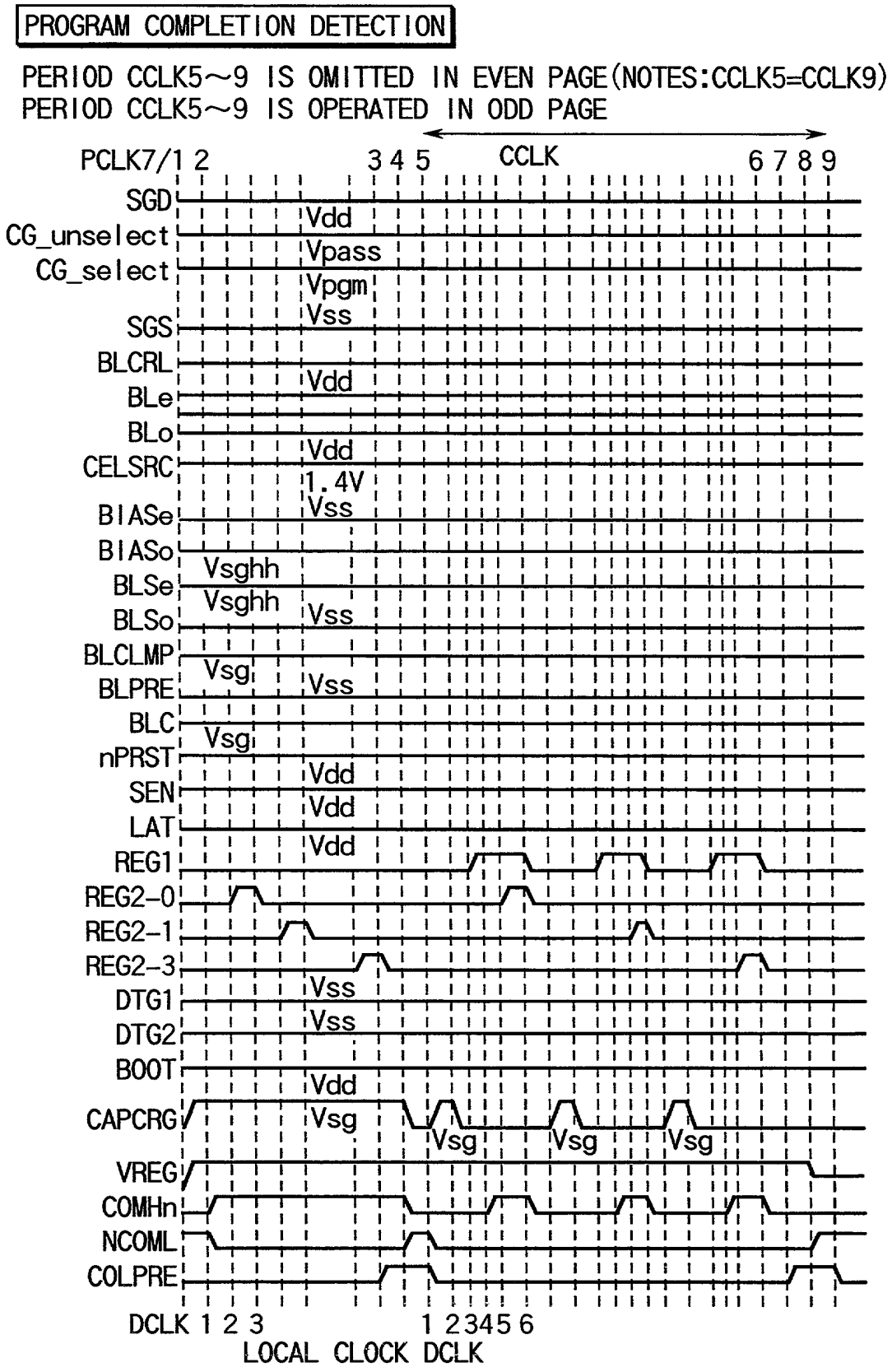
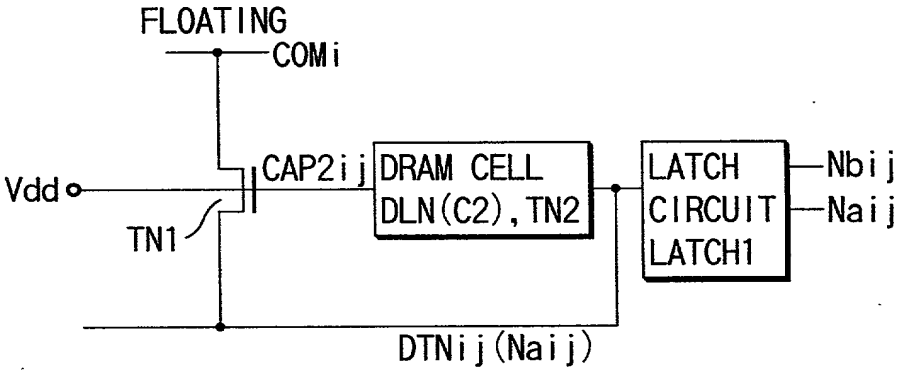

PROGRAM COMPLETION DETECTION
PERIOD CCLK5~9 IS OMITTED IN EVEN PAGE(NOTES:CCLK5=CCLK9)
PERIOD CCLK5~9 IS OPERATED IN ODD PAGE
PCLK7/1 2 3 4 5 CCLK 6 7 8 9
SGD
CG_unselect
CG_select
SGS
BLCRL
BLe
BLo
CELSRC
BIASe
BIASo
BLSe
BLSo
BLCLMP
BLPRE
BLC
nPRST
SEN
LAT
REG1
REG2-0
REG2-1
REG2-3
DTG1
DTG2
BOOT
CAPCRG
VREG
COMHn
NCOML
COLPRE
Vdd
Vpass
Vpgm
Vss
1.4V
Vsghh
Vsg
DCLK 1 2 3 1 2 3 4 5 6
LOCAL CLOCK DCLK

FIG. 33

PROGRAM OF EVEN PAGE DATA (PROGRAM COMPLETION DETECTION)



DTNij(Naij)	H	L
COMi	H	L
	↓	↓
	"10"-PROGRAMMING SUFFICIENT	"10"-PROGRAMMING DEFFICIENT

FIG. 34

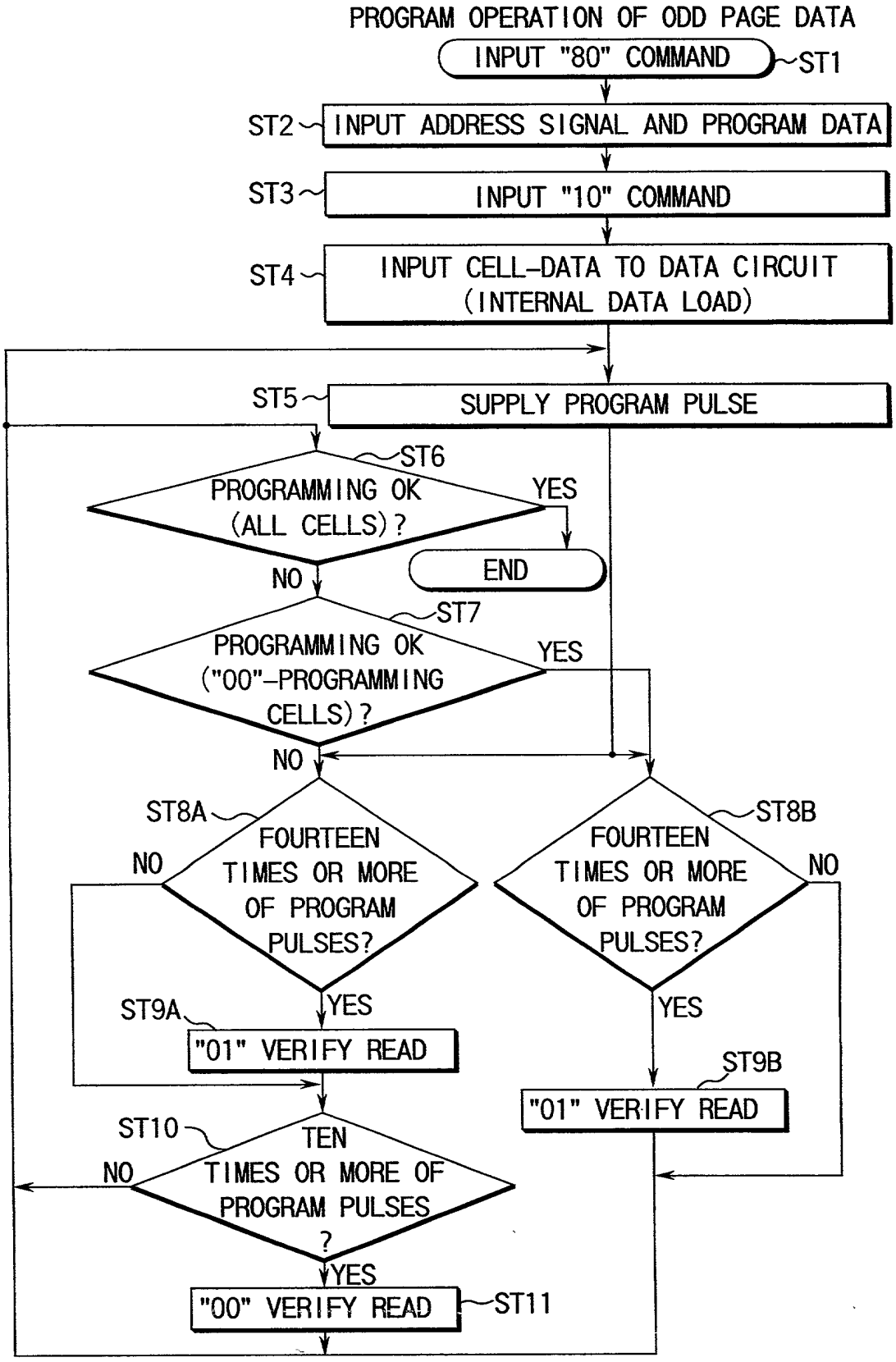

PROGRAM OPERATION OF ODD PAGE DATA
INPUT "80" COMMAND
ST1
ST2
INPUT ADDRESS SIGNAL AND PROGRAM DATA
ST3
INPUT "10" COMMAND
ST4
INPUT CELL-DATA TO DATA CIRCUIT (INTERNAL DATA LOAD)
ST5
SUPPLY PROGRAM PULSE
ST6
PROGRAMMING OK (ALL CELLS)?
YES
END
NO
ST7
PROGRAMMING OK ("00"-PROGRAMMING CELLS)?
YES
NO
ST8A
FOURTEEN TIMES OR MORE OF PROGRAM PULSES?
NO
YES
ST8B
FOURTEEN TIMES OR MORE OF PROGRAM PULSES?
NO
YES
ST9A
"01" VERIFY READ
ST9B
"01" VERIFY READ
ST10
TEN TIMES OR MORE OF PROGRAM PULSES ?
NO
YES
"00" VERIFY READ
ST11

FIG. 35

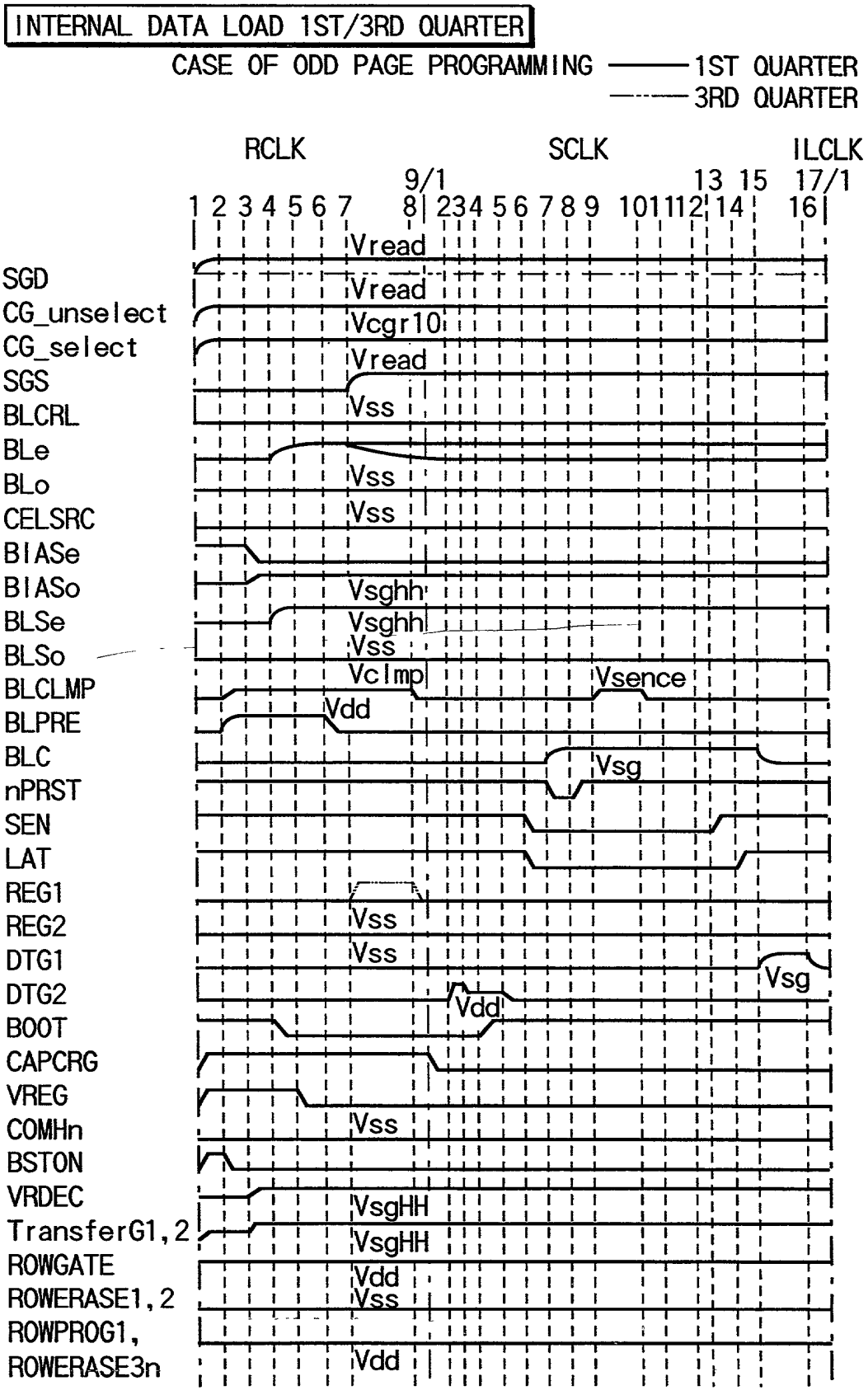


FIG. 36

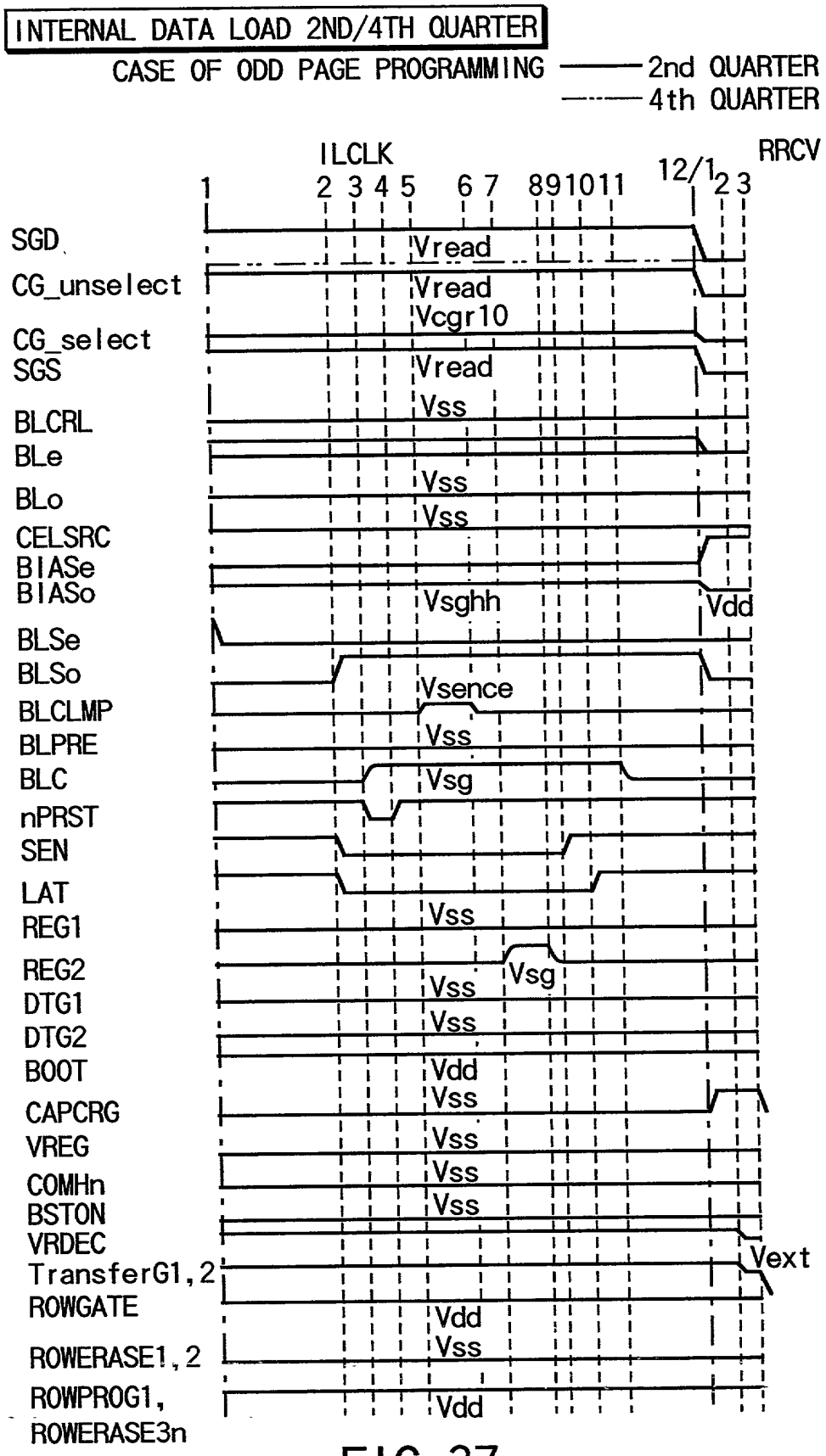

INTERNAL DATA LOAD 2ND/4TH QUARTER
CASE OF ODD PAGE PROGRAMMING
2nd QUARTER
4th QUARTER
ILCLK
RRCV
1
2 3 4 5 6 7 8 9 10 11
12/1
2 3
SGD
CG_unselect
CG_select
SGS
BLCRL
BLe
BLo
CELSRC
BIASe
BIASo
BLSe
BLSo
BLCLMP
BLPRE
BLC
nPRST
SEN
LAT
REG1
REG2
DTG1
DTG2
BOOT
CAPCRG
VREG
COMHn
BSTON
VRDEC
TransferG1, 2
ROWGATE
ROWERASE1, 2
ROWPROG1,
ROWERASE3n
Vread
Vcgr10
Vss
Vsghh
Vdd
Vsence
Vsg
Vext

FIG. 37

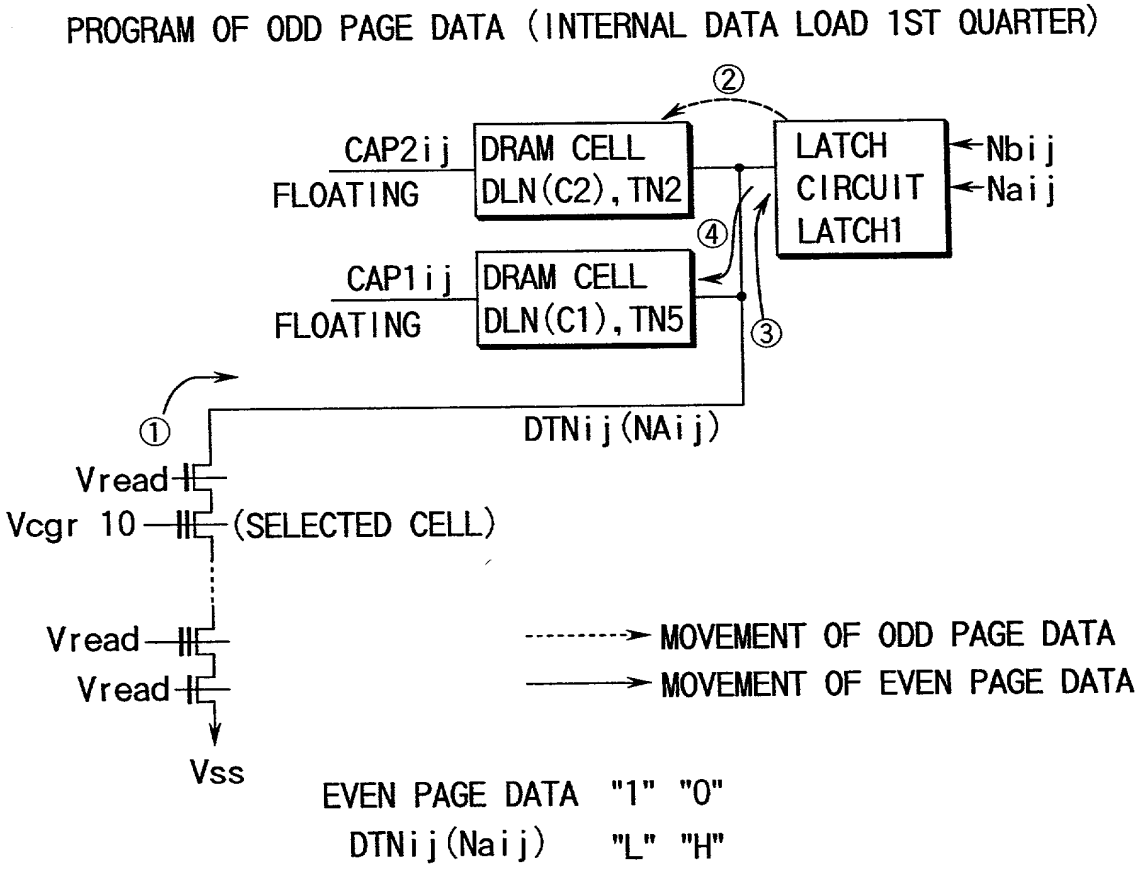
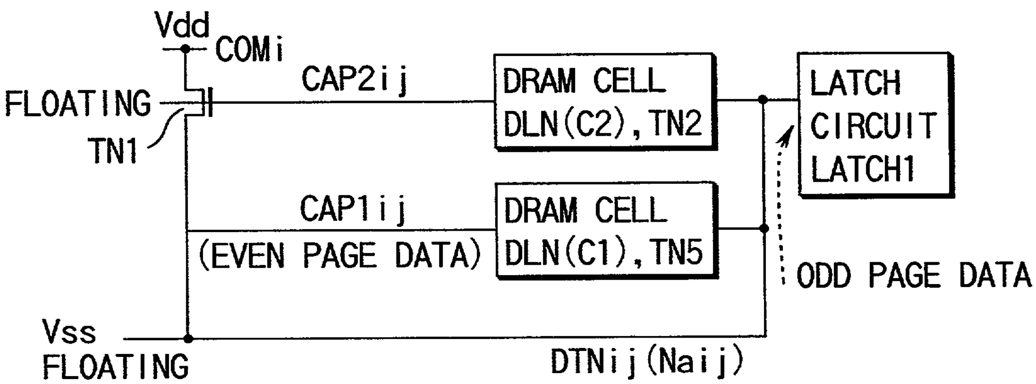


FIG. 38

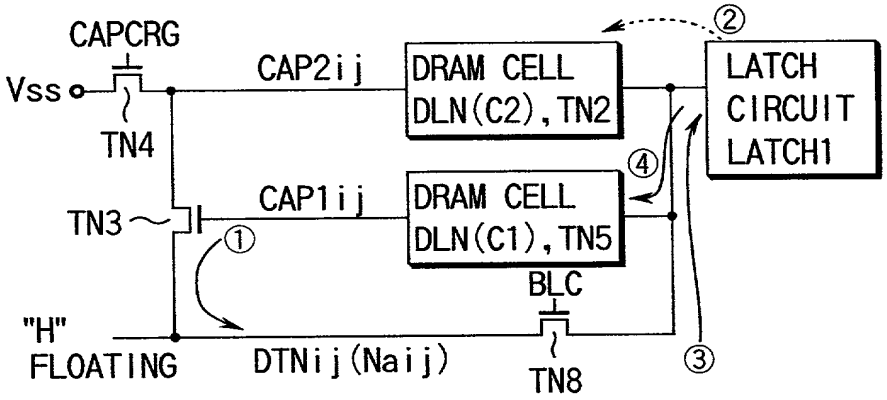
PROGRAM OF ODD PAGE DATA (INTERNAL DATA LOAD 2ND QUARTER)



ODD PAGE DATA	"1"	"0"
CAP2ij	"H"	"L"
DTNij	"H"	"L"
EVEN PAGE DATA	"1"	"0"
CAP1ij	"L"	"H"

FIG. 39

PROGRAM OF ODD PAGE DATA (INTERNAL DATA LOAD 3RD QUARTER)



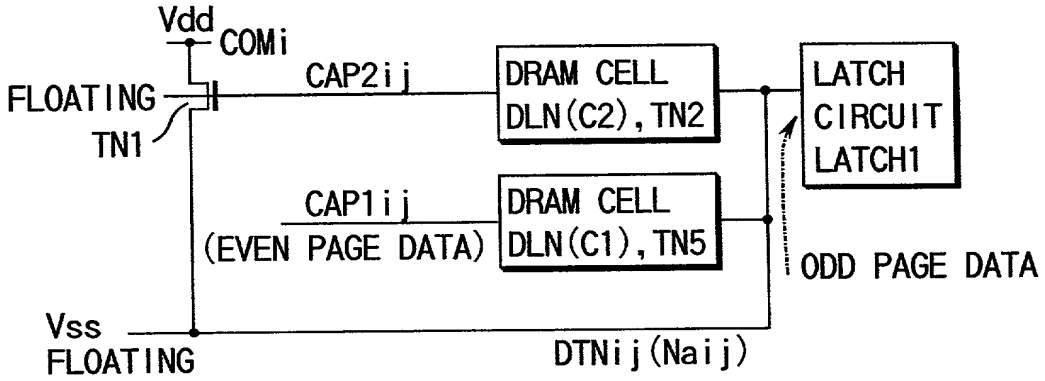
EVEN PAGE DATA	"1" "0"
CAP1ij	"L" "H"
DTNij	"H" "L"

⋯⋯→ MOVEMENT OF ODD PAGE DATA

——→ MOVEMENT OF EVEN PAGE DATA

FIG. 40

PROGRAM OF ODD PAGE DATA (INTERNAL DATA LOAD 4TH QUARTER)



ODD PAGE DATA	"1"	"0"
CAP2ij	"H"	"L"
DTNij	"H"	"L"
EVEN PAGE DATA	"1"	"0"
CAP1ij	"H"	"L"

FIG. 41

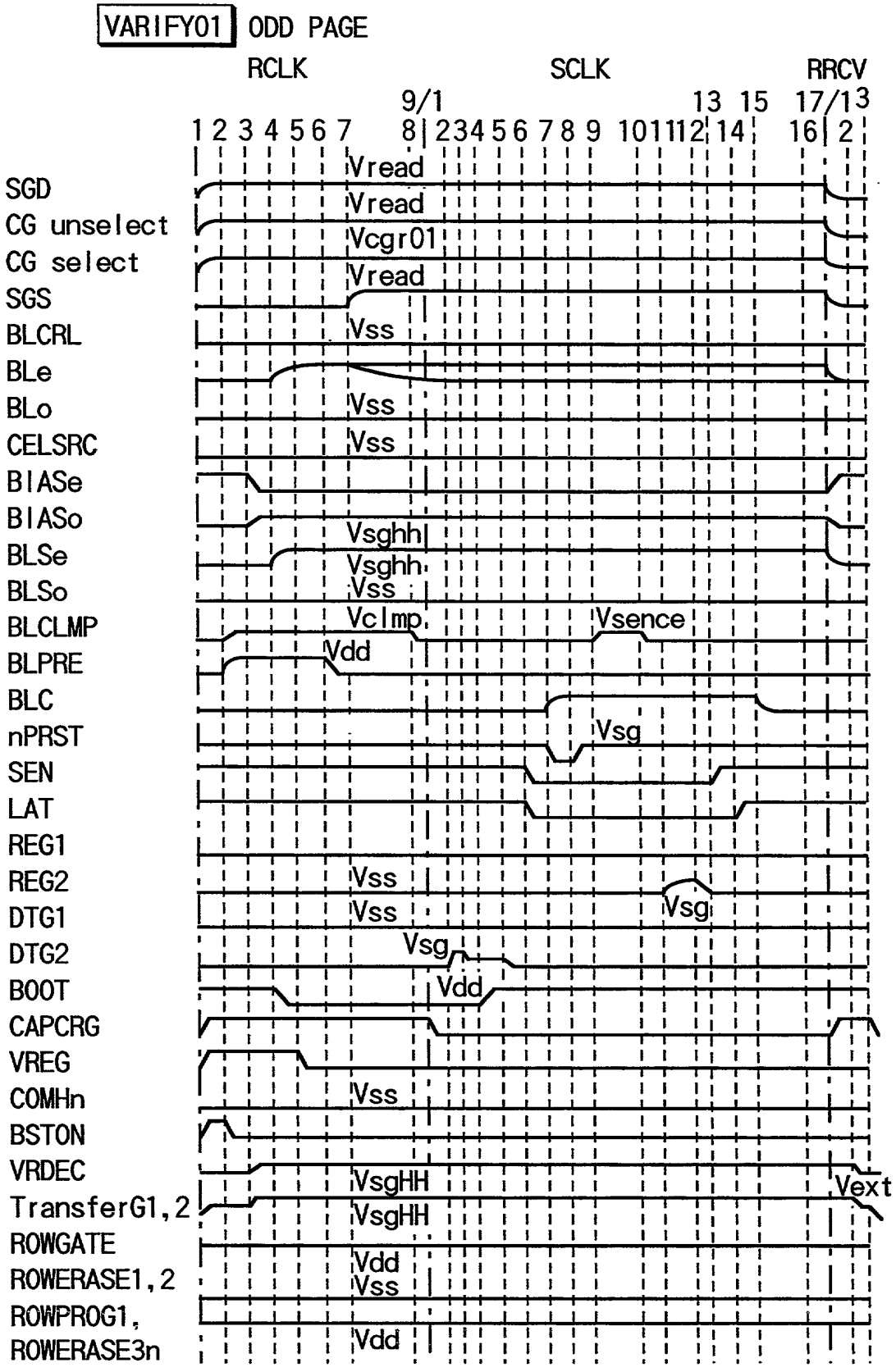
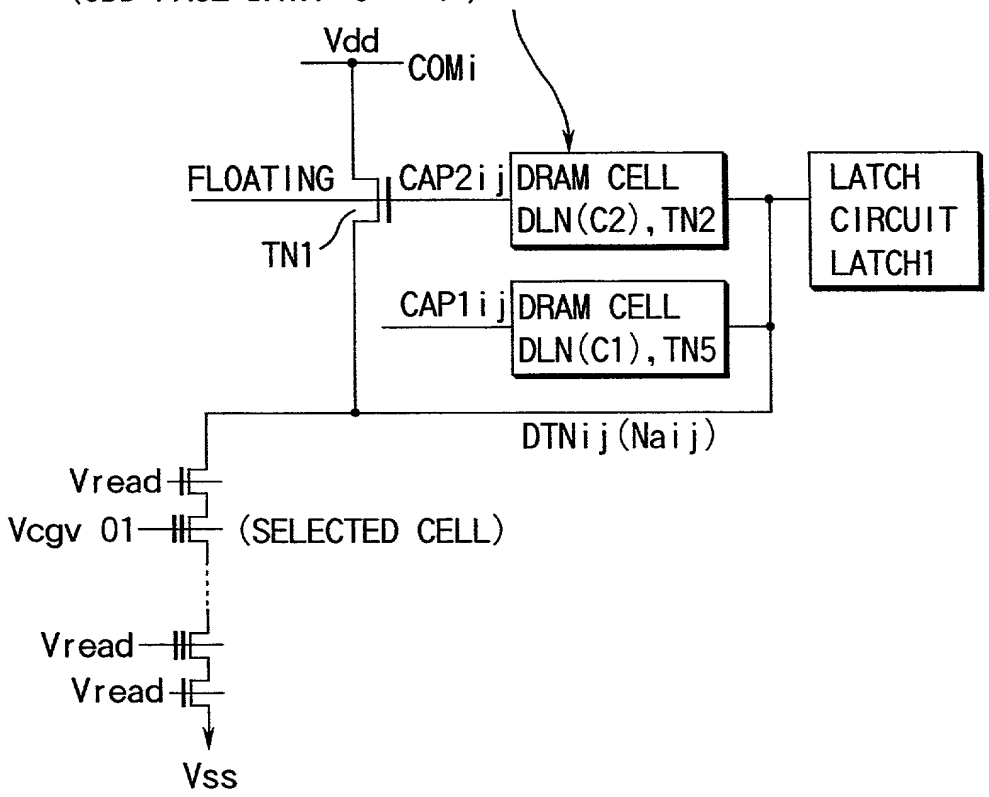

VARIFY01
ODD PAGE
RCLK
SCLK
RRCV
9/1
13 15
17/13
1 2 3 4 5 6 7 8 2 3 4 5 6 7 8 9 10 11 12 14 16 2
SGD
CG unselect
CG select
SGS
BLCRL
BLe
BLo
CELSRC
BIASe
BIASo
BLSe
BLSo
BLCLMP
BLPRE
BLC
nPRST
SEN
LAT
REG1
REG2
DTG1
DTG2
BOOT
CAPCRG
VREG
COMHn
BSTON
VRDEC
TransferG1,2
ROWGATE
ROWERASE1,2
ROWPROG1,
ROWERASE3n
Vread
Vread
Vcgr01
Vread
Vss
Vss
Vss
Vsghh
Vsghh
Vss
Vclmp
Vsence
Vdd
Vsg
Vss
Vss
Vsg
Vsg
Vdd
Vss
VsgHH
VsgHH
Vdd
Vss
Vdd
Vext

FIG. 42

PROGRAM OF ODD PAGE DATA ("01" VERIFY READ)

- "11","10"-PROGRAMMING→"H"(ODD PAGE DATA "1")
- "00","01"-PROGRAMMING (DEFICIENT)→"L"(ODD PAGE DATA "0")
- "01"-PROGRAMMING (SUFFICIENT)→"H"(ODD PAGE DATA "0"→"1")

*"00"-PROGRAMMING (SUFFICIENT)→"10"-PROGRAMMING (ODD PAGE DATA "0"→"1")



	"11","10"-PROGRAMMING	"00"-PROGRAMMING		"01"-PROGRAMMING	
STATE OF SELECTED CELL	"11","10"	"00" DEFICIENT	"00" SUFFICIENT	"01" DEFICIENT	"01" SUFFICIENT
BIT LINE	L	L	L	L	H
DTNij(Naij)	H	L	H	L	H

NO DATA CHANGE

CHANGE OF ODD PAGE DATA "0"→"1"

TO LATCH CIRCUIT LATCH1

FIG. 43

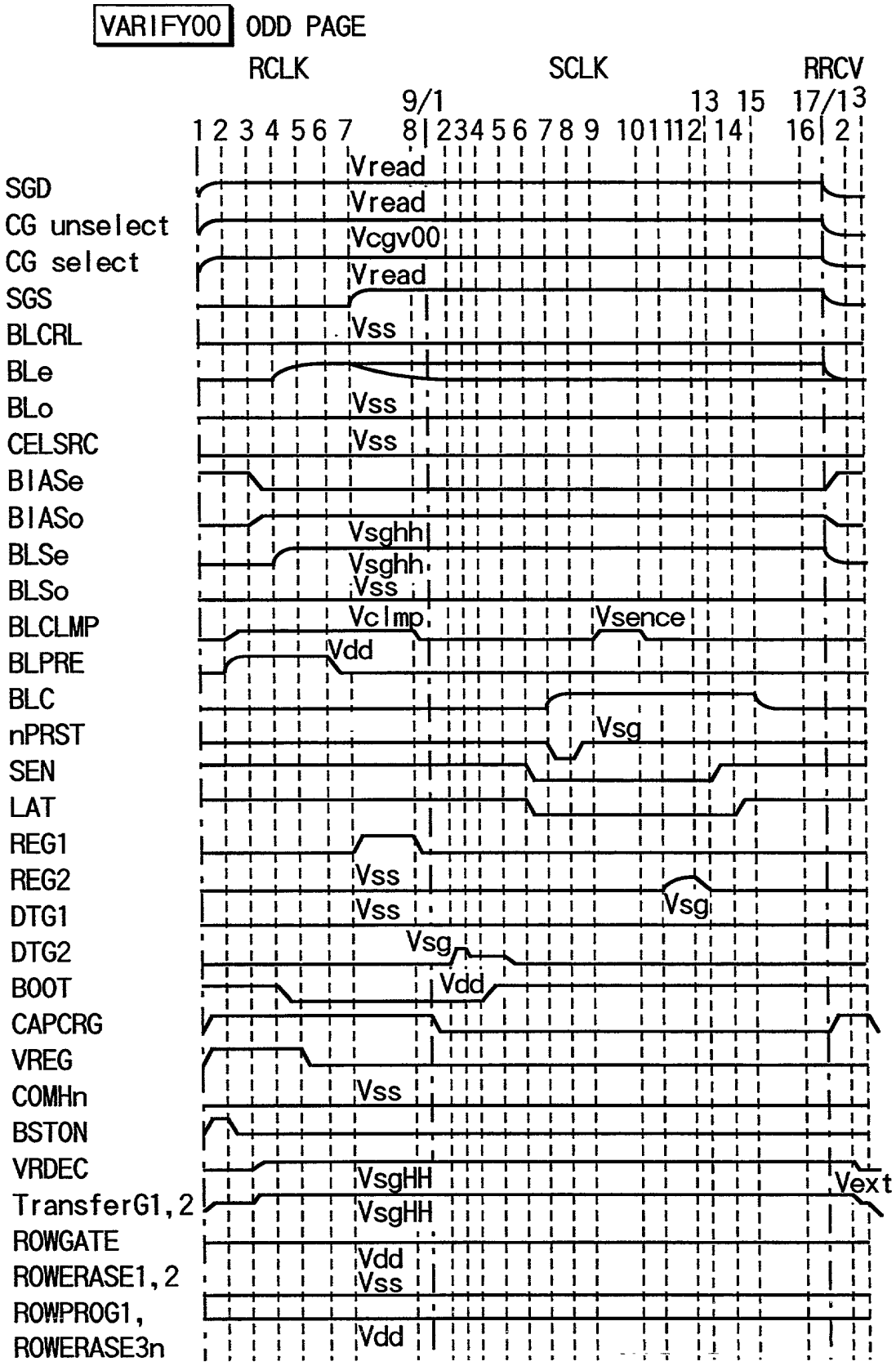
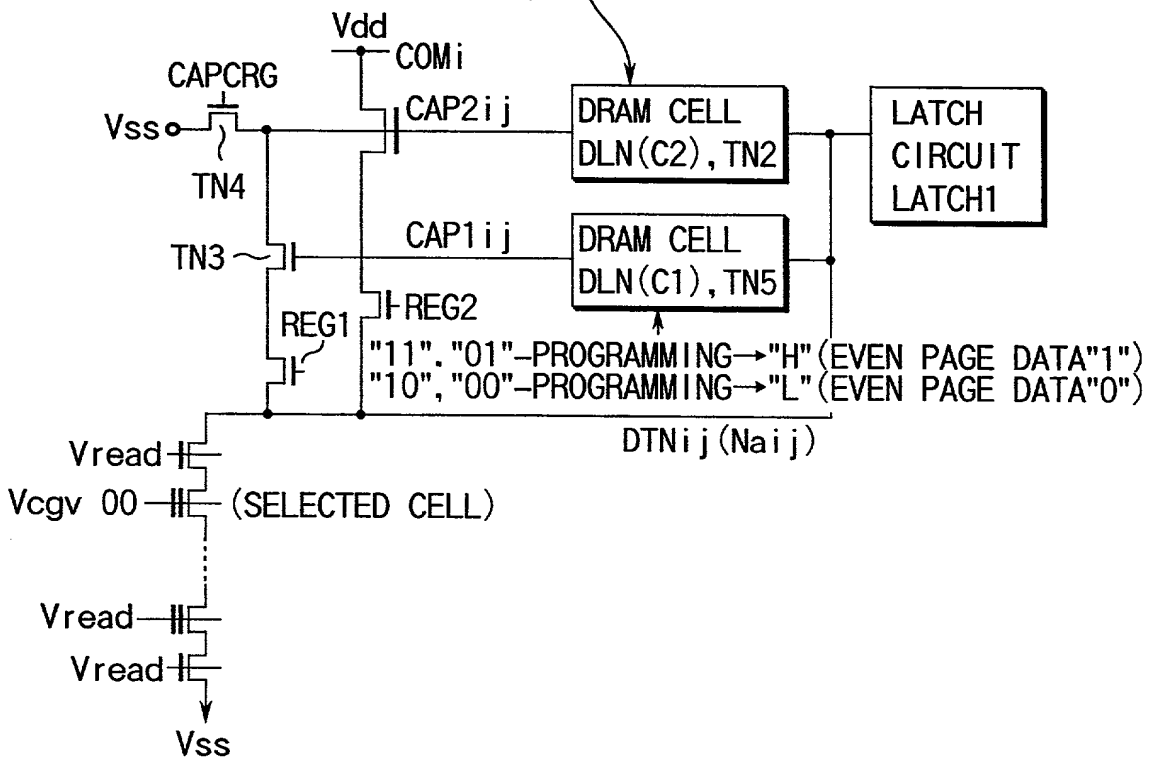

VARIFY00
ODD PAGE
RCLK
SCLK
RRCV
9/1
13 15
17/13
1 2 3 4 5 6 7 8 2 3 4 5 6 7 8 9 10 11 12 14 16 2
SGD
CG unselect
CG select
SGS
BLCRL
BLe
BLo
CELSRC
BIASe
BIASo
BLSe
BLSo
BLCLMP
BLPRE
BLC
nPRST
SEN
LAT
REG1
REG2
DTG1
DTG2
BOOT
CAPCRG
VREG
COMHn
BSTON
VRDEC
TransferG1,2
ROWGATE
ROWERASE1,2
ROWPROG1,
ROWERASE3n
Vread
Vcgv00
Vss
Vsghh
Vclmp
Vsence
Vdd
Vsg
VsgHH
Vext

FIG. 44

PROGRAM OF ODD PAGE DATA ("00" VERIFY READ)

- "11","10"-PROGRAMMING→"H"(ODD PAGE DATA "1")
- "00","01"-PROGRAMMING (DEFICIENT)→"L"(ODD PAGE DATA "0")
- "00"-PROGRAMMING (SUFFICIENT)→"H"(ODD PAGE DATA "0"→"1")

*"01"-PROGRAMMING (SUFFICIENT)→"11"-PROGRAMMING (ODD PAGE DATA "0"→"1")



	"11","10"-PROGRAMMING	"00"-PROGRAMMING		"01"-PROGRAMMING	
STATE OF SELECTED CELL	"11","10"	"00" DEFICIENT	"00" SUFFICIENT	"01" DEFICIENT	"01" SUFFICIENT
BIT LINE	L L	L	H	H OR L	H
DTNij (PERIOD REG1="H")	L L	L	H	L	L
DTNij (PERIOD REG2="H")	H	L	H	L	H
	NO DATA CHANGE		CHANGE OF ODD PAGE DATA "0"→"1"	NO DATA CHANGE	TO LATCH CIRCUIT LATCH1

FIG. 45

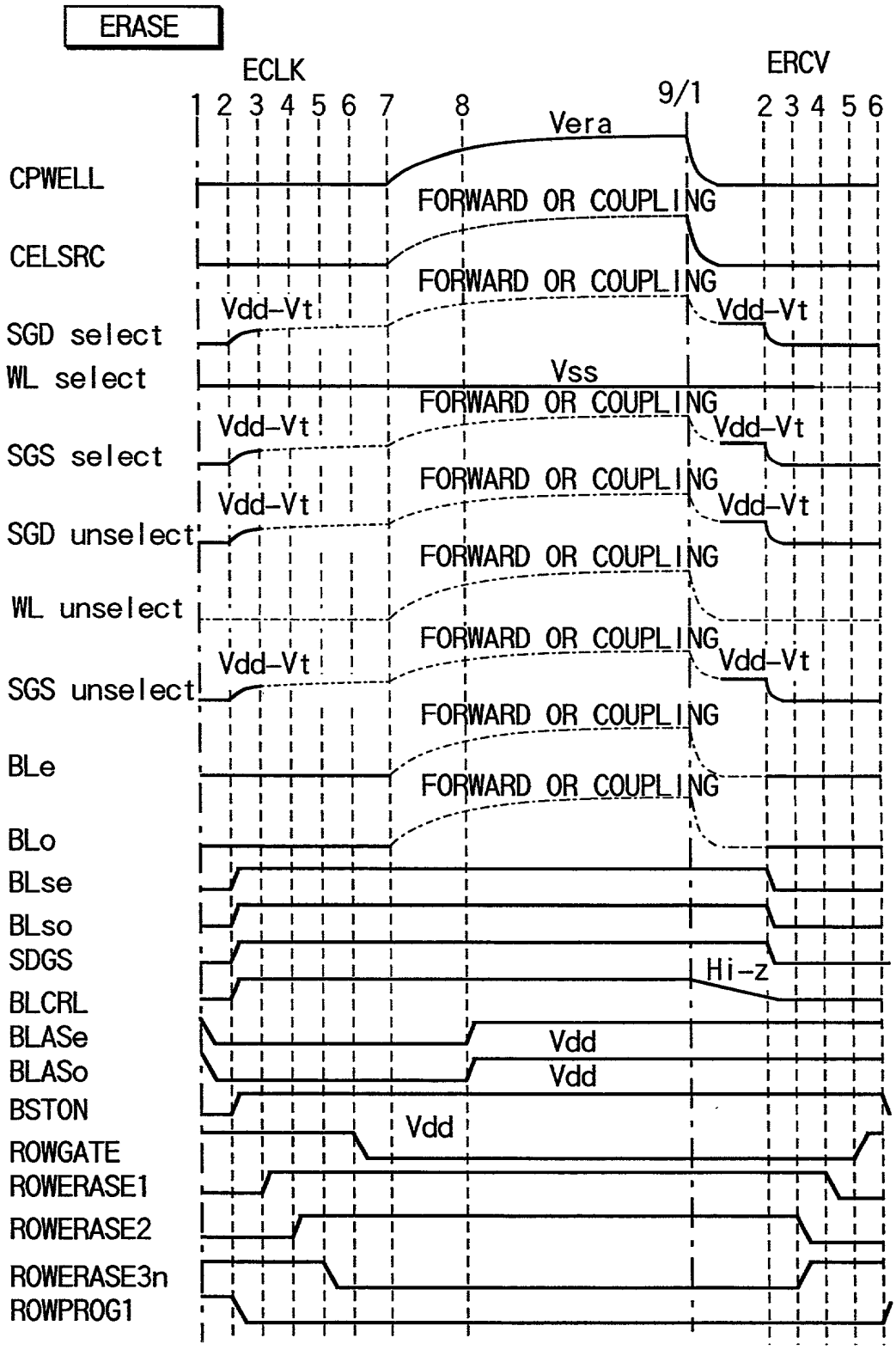

ERASE
ECLK
ERCV
1 2 3 4 5 6 7 8 9/1 2 3 4 5 6
Vera
CPWELL
FORWARD OR COUPLING
CELSRC
FORWARD OR COUPLING
Vdd-Vt
Vdd-Vt
SGD select
WL select
Vss
FORWARD OR COUPLING
Vdd-Vt
Vdd-Vt
SGS select
FORWARD OR COUPLING
Vdd-Vt
Vdd-Vt
SGD unselect
FORWARD OR COUPLING
WL unselect
FORWARD OR COUPLING
Vdd-Vt
Vdd-Vt
SGS unselect
FORWARD OR COUPLING
BLe
FORWARD OR COUPLING
BLo
BLse
BLso
SDGS
Hi-z
BLCRL
BLASe
Vdd
BLASo
Vdd
BSTON
Vdd
ROWGATE
ROWERASE1
ROWERASE2
ROWERASE3n
ROWPROG1

FIG. 46

ERASE VERIFY READ

VERIFY OF EVEN COLUMN→ALL DETECTION→DETECTION OF FAIL CELL NUMBER(Y-SCAN)→VERIFY OF ODD COLUMN→ALL DETECTION →DETECTION OF FAIL CELL NUMBER(Y-SCAN)

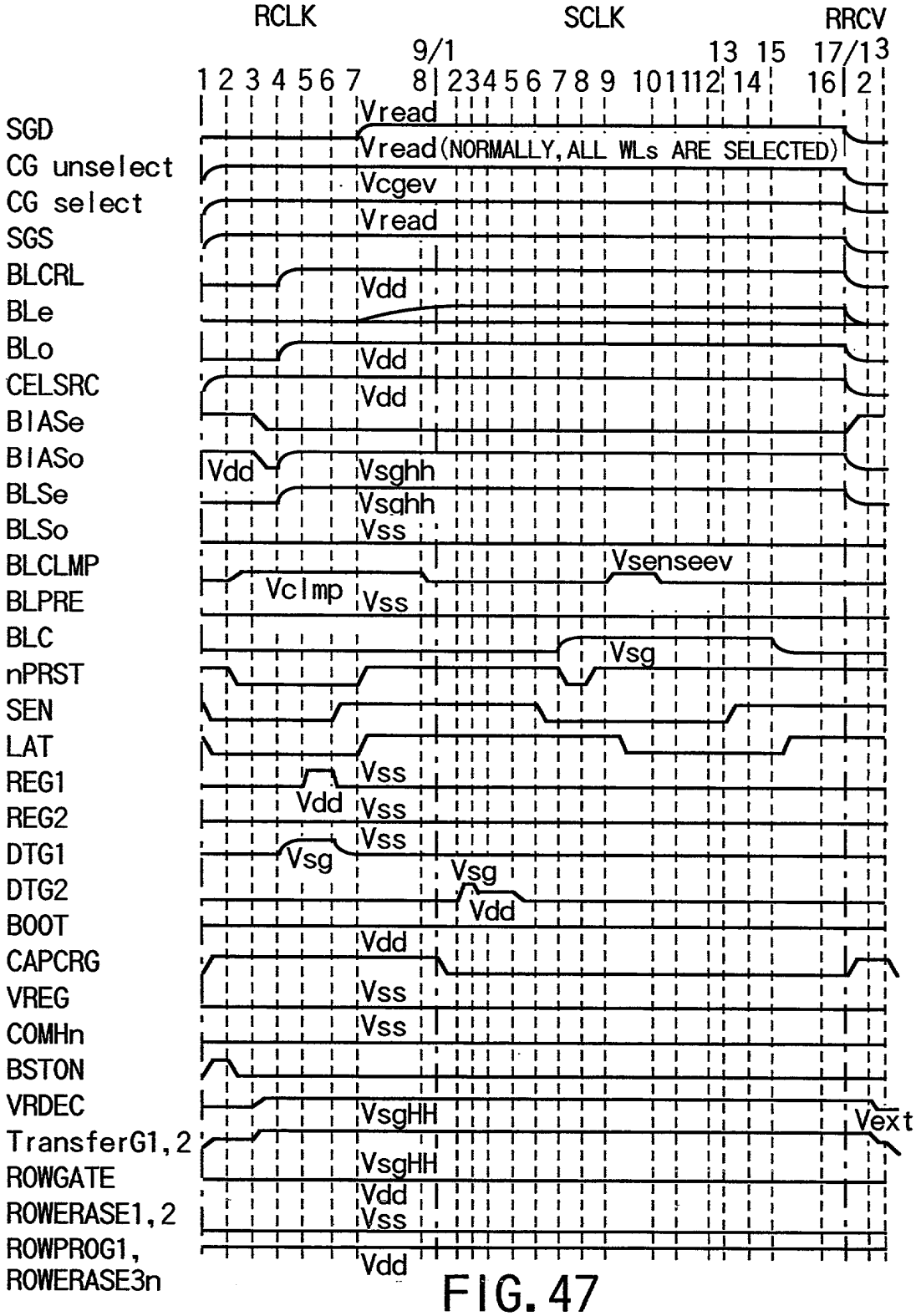


FIG. 47

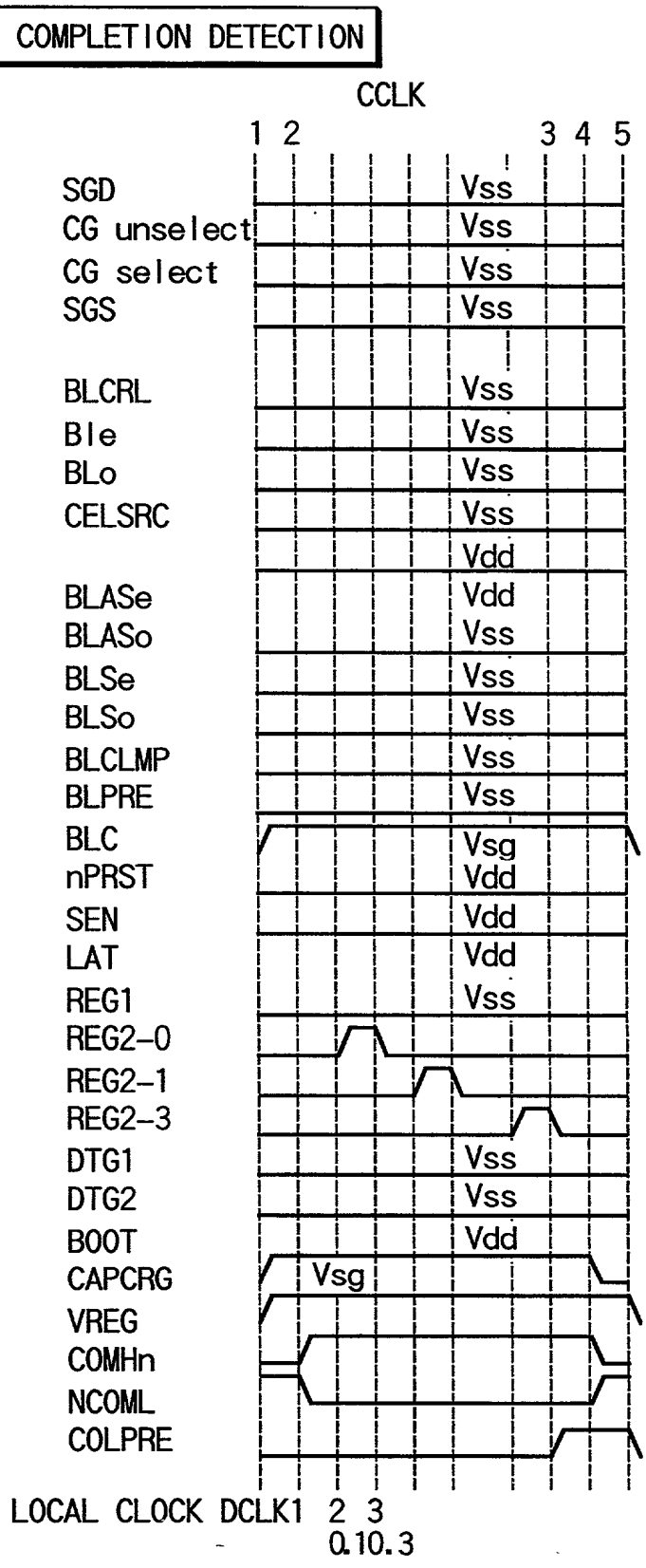

ERASE COMPLETION DETECTION
CCLK
1 2 3 4 5
SGD
CG unselect
CG select
SGS
BLCRL
Ble
BLo
CELSRC
BLASe
BLASo
BLSe
BLSo
BLCLMP
BLPRE
BLC
nPRST
SEN
LAT
REG1
REG2-0
REG2-1
REG2-3
DTG1
DTG2
BOOT
CAPCRG
VREG
COMHn
NCOML
COLPRE
Vss
Vdd
Vsg
LOCAL CLOCK DCLK1 2 3
0.1 0.3

FIG. 48

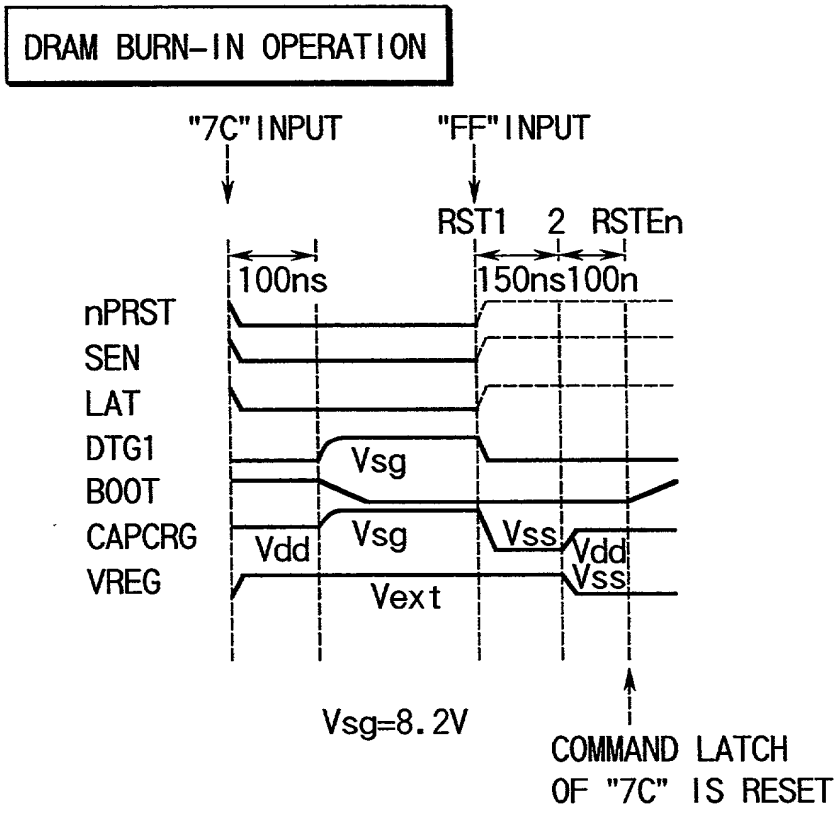


FIG. 49

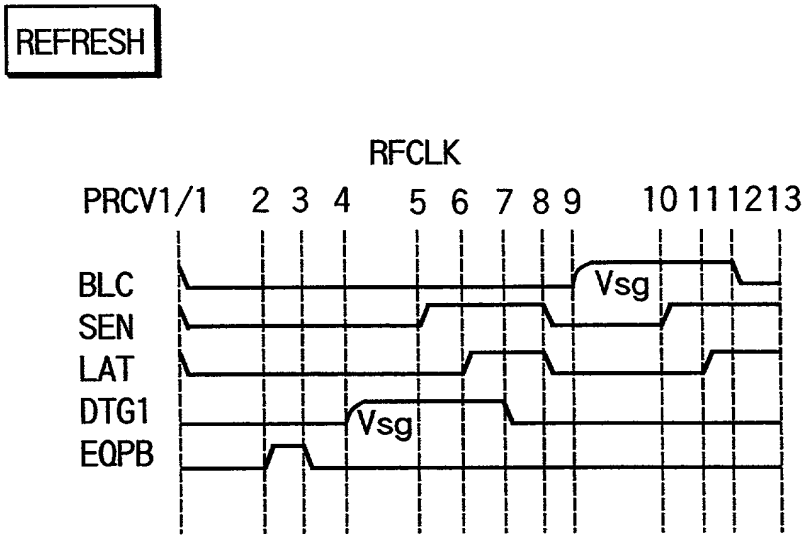


FIG. 50

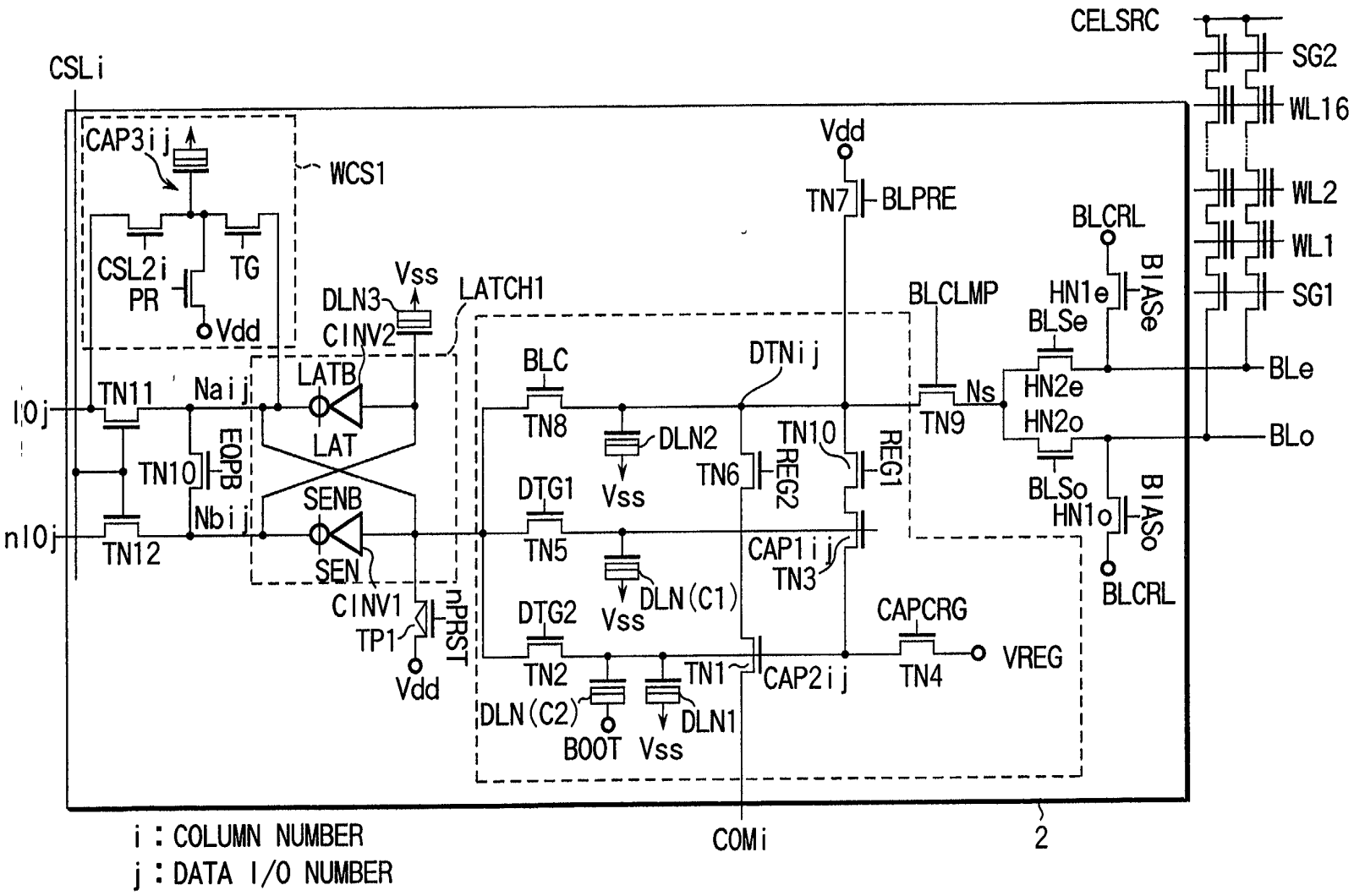

CELSRC
SG2
WL16
WL2
WL1
SG1
CSLi
CAP3ij
WCS1
Vdd
TN7
BLPRE
BLCRL
BIASe
CSL2i
PR
TG
Vdd
Vss
DLN3
CINV2
LATCH1
BLCLMP
HN1e
BLSe
BLe
BLC
DTNij
LATB
TN11
Naij
I/Oj
LAT
TN8
DLN2
TN10
REG1
TN9
Ns
HN2e
HN2o
BLo
EQPB
TN10
DTG1
Vss
TN6
REG2
BLSo
BIASo
HN1o
SENB
Nbij
nI/Oj
TN12
TN5
CAP1ij
TN3
SEN
CINV1
nPRST
DTG2
Vss
DLN(C1)
CAPCRG
BLCRL
TP1
Vdd
TN2
TN1
CAP2ij
TN4
VREG
DLN(C2)
DLN1
BOOT
Vss
i : COLUMN NUMBER
j : DATA I/O NUMBER
COMi
2

FIG. 51

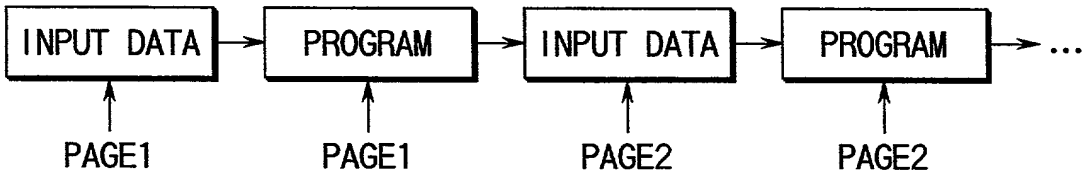

INPUT DATA
PROGRAM
INPUT DATA
PROGRAM
PAGE1
PAGE1
PAGE2
PAGE2

FIG. 52

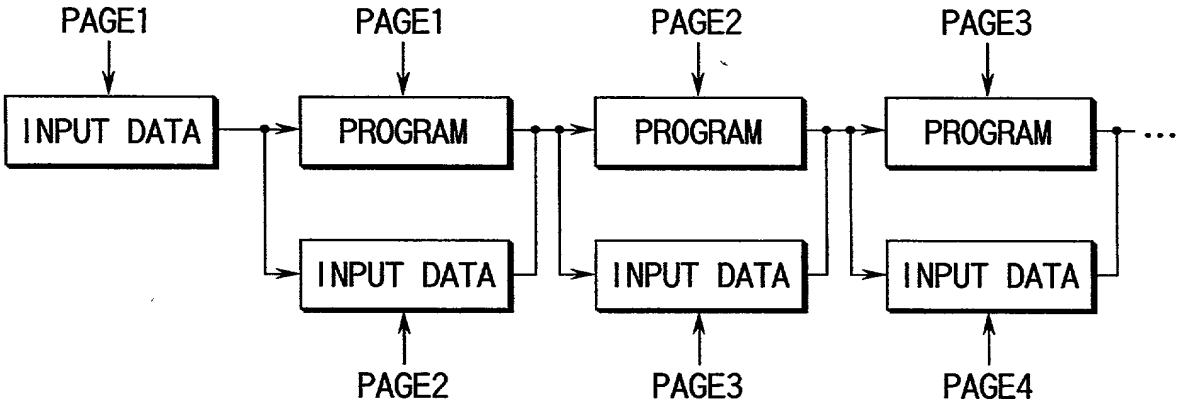

PAGE1
PAGE1
PAGE2
PAGE3
INPUT DATA
PROGRAM
PROGRAM
PROGRAM
INPUT DATA
INPUT DATA
INPUT DATA
PAGE2
PAGE3
PAGE4

FIG. 53

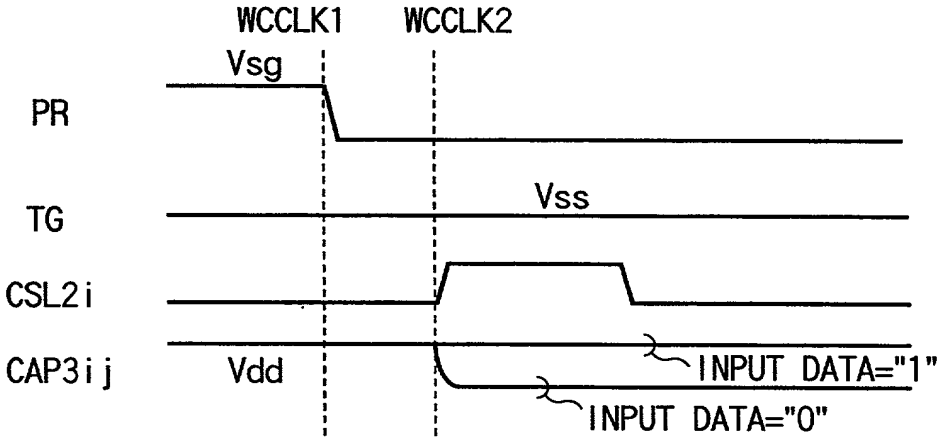


FIG. 54

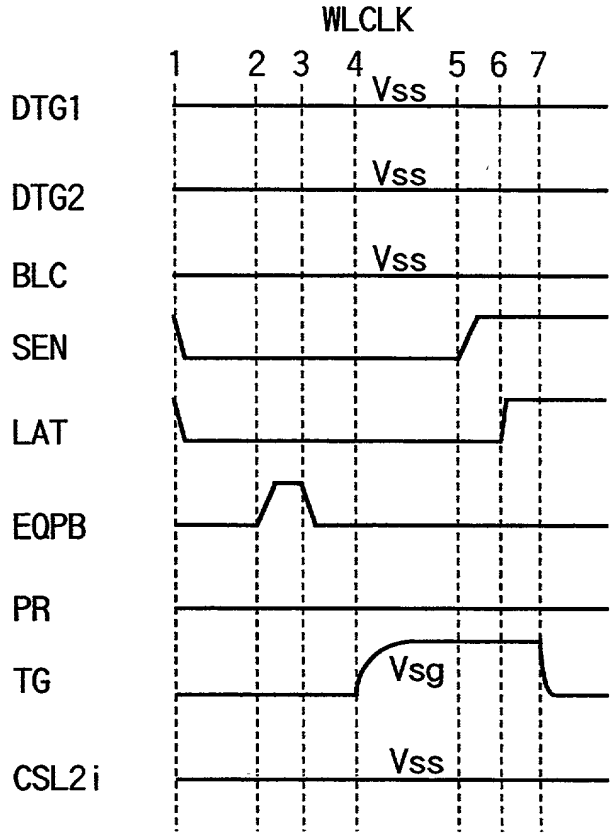


FIG. 55

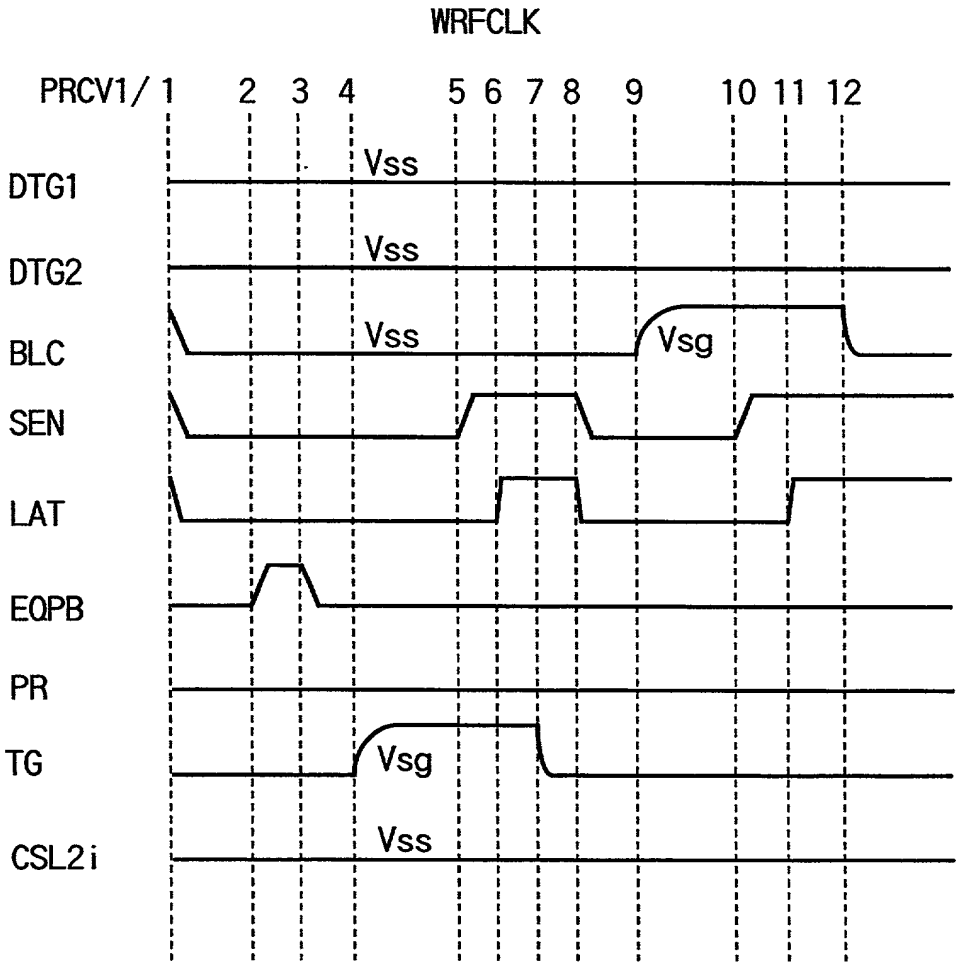

WRFCLK
PRCV1/
1
2
3
4
5
6
7
8
9
10
11
12
DTG1
Vss
DTG2
Vss
BLC
Vss
Vsg
SEN
LAT
EQPB
PR
TG
Vsg
CSL2i
Vss

FIG. 56

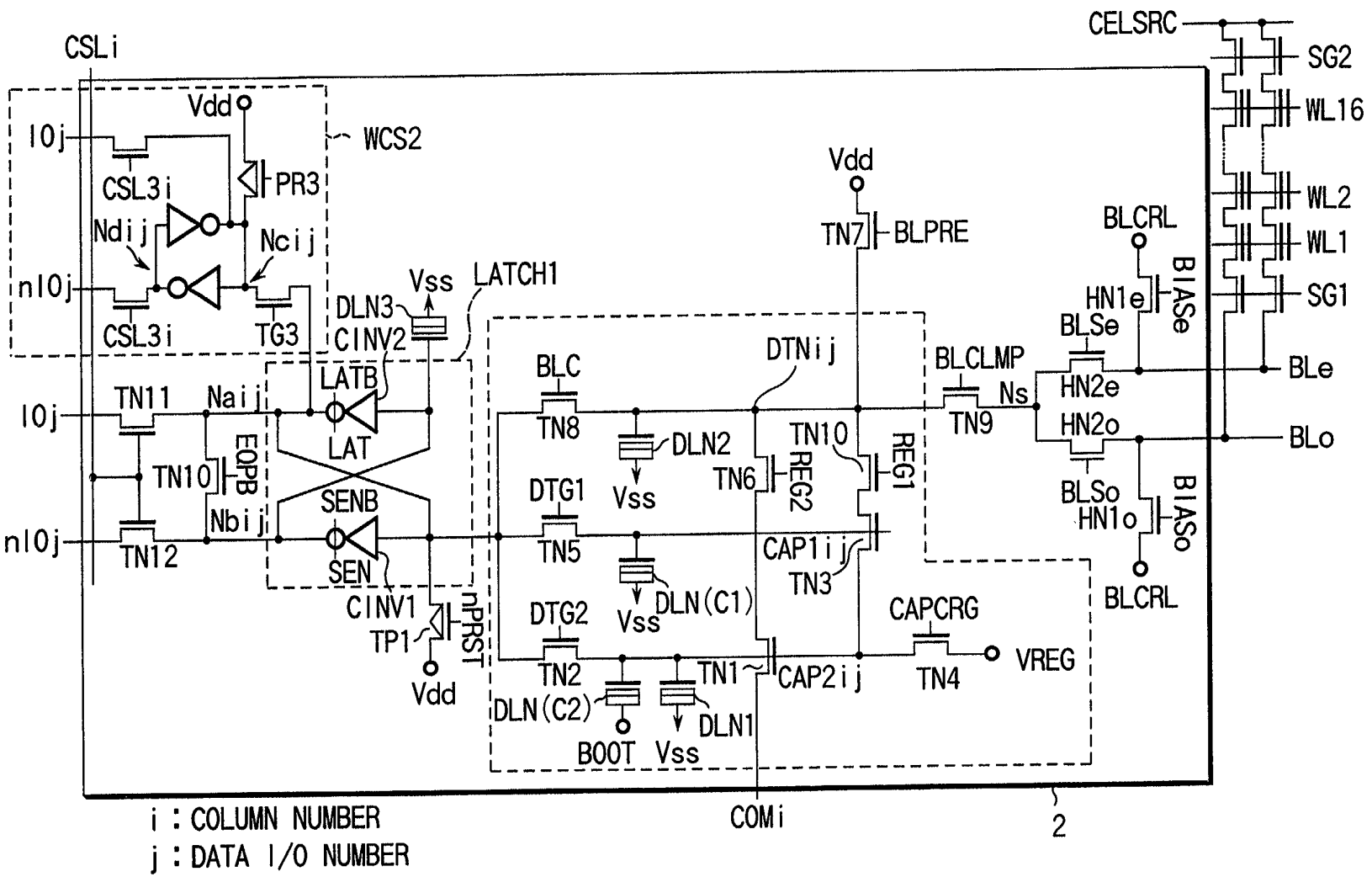

CSLi
CELSRC
SG2
WL16
WL2
WL1
SG1
BLe
BLo
Vdd
WCS2
I0j
CSL3i
PR3
Ndij
Ncij
nI0j
CSL3i
TG3
Vss
LATCH1
DLN3
CINV2
LATB
LAT
TN11
Naij
I0j
TN10
EQPB
Nbij
nI0j
TN12
SENB
SEN
CINV1
TP1
nPRST
Vdd
BLC
TN8
DLN2
Vss
DTG1
TN5
DTG2
TN2
DLN(C2)
BOOT
Vss
DLN(C1)
Vss
DTNij
TN10
REG1
TN6
REG2
CAP1ij
TN3
TN1
CAP2ij
DLN1
Vss
Vdd
TN7
BLPRE
BLCLMP
Ns
TN9
CAPCRG
TN4
VREG
BLCRL
HN1e
BIASe
BLSe
HN2e
HN2o
BLSo
HN1o
BIASo
BLCRL
i : COLUMN NUMBER
j : DATA I/O NUMBER
COMi
2

FIG. 57

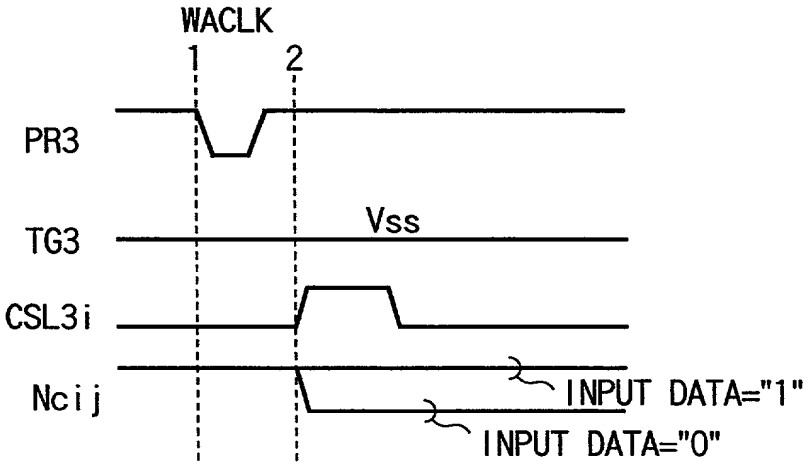

WACLK
1
2
PR3
TG3
Vss
CSL3i
Ncij
INPUT DATA="1"
INPUT DATA="0"

FIG. 58

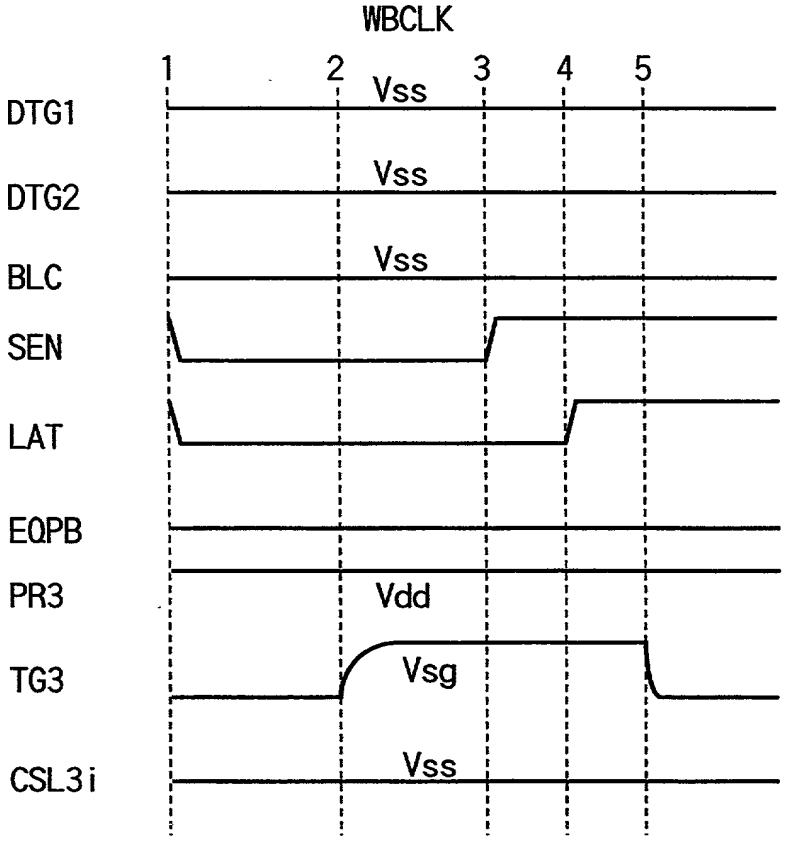

WBCLK
1
2
3
4
5
DTG1
Vss
DTG2
Vss
BLC
Vss
SEN
LAT
EQPB
PR3
Vdd
TG3
Vsg
CSL3i
Vss

FIG. 59

FIG. 60A

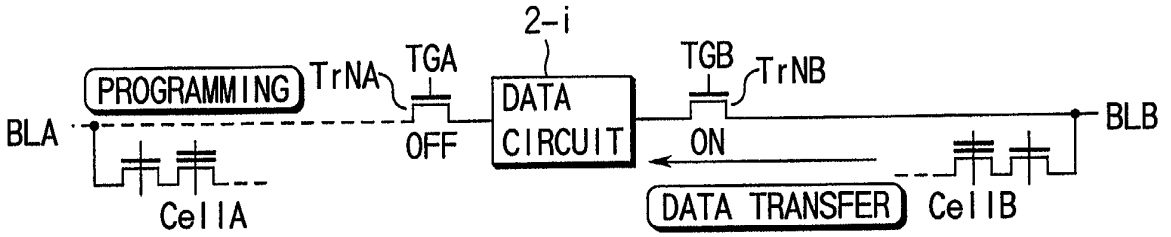


FIG. 60B

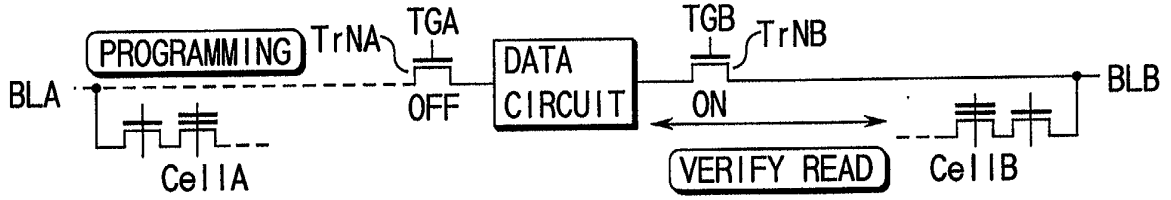


FIG. 60C

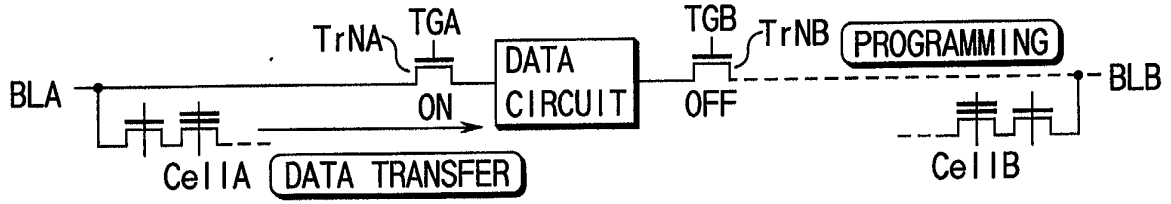
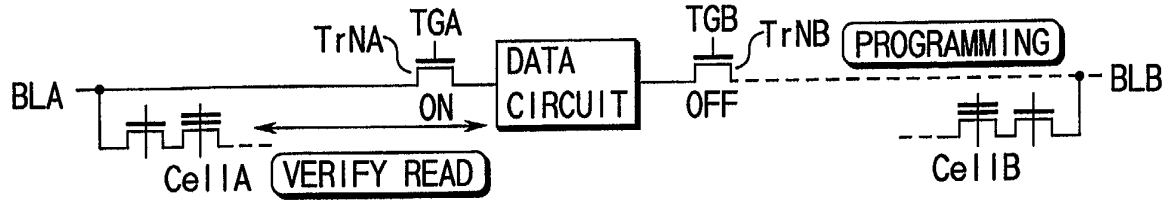


FIG. 60D



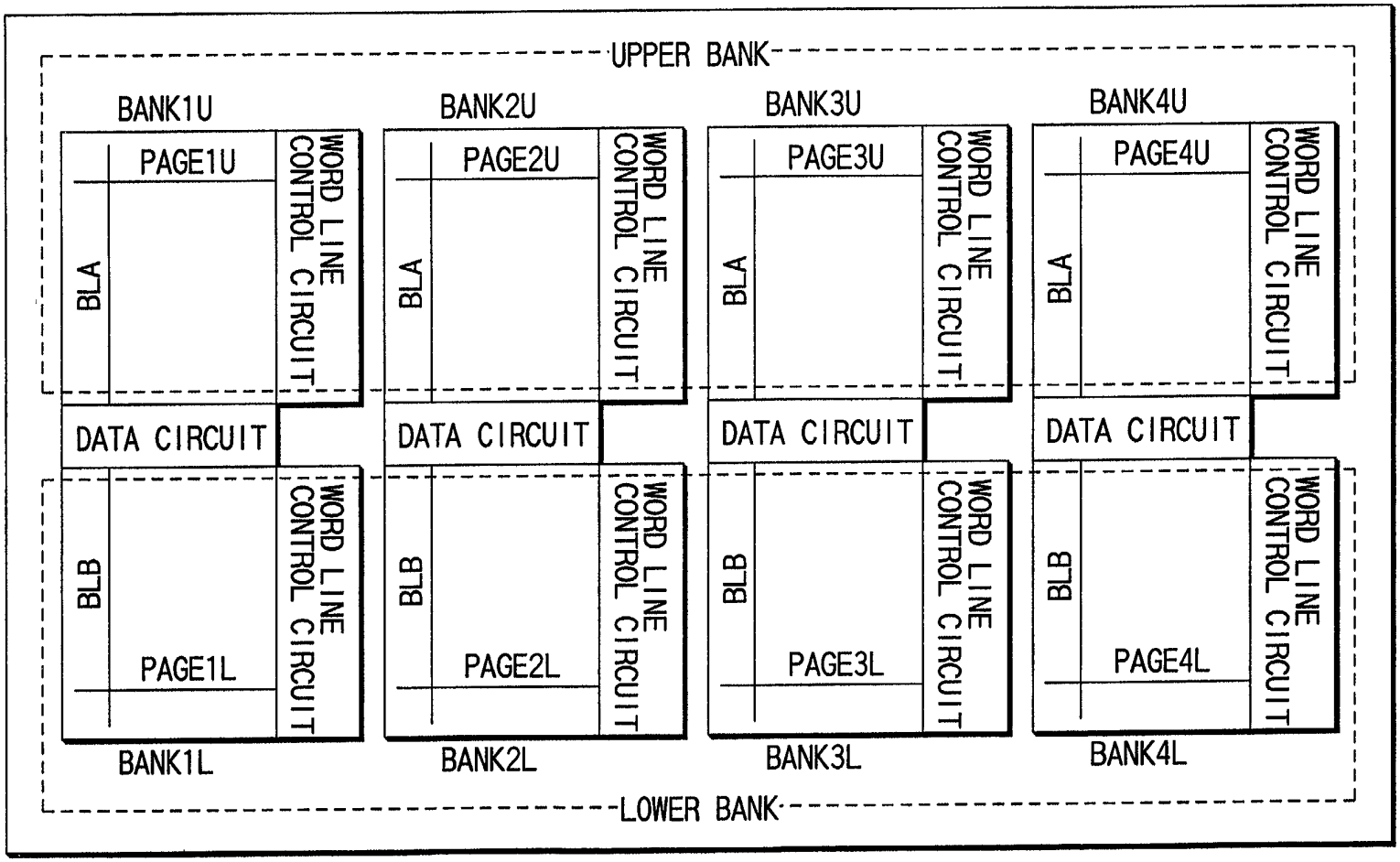

UPPER BANK
BANK1U
BANK2U
BANK3U
BANK4U
PAGE1U
PAGE2U
PAGE3U
PAGE4U
BLA
WORD LINE CONTROL CIRCUIT
DATA CIRCUIT
BLB
PAGE1L
PAGE2L
PAGE3L
PAGE4L
BANK1L
BANK2L
BANK3L
BANK4L
LOWER BANK

FIG. 61

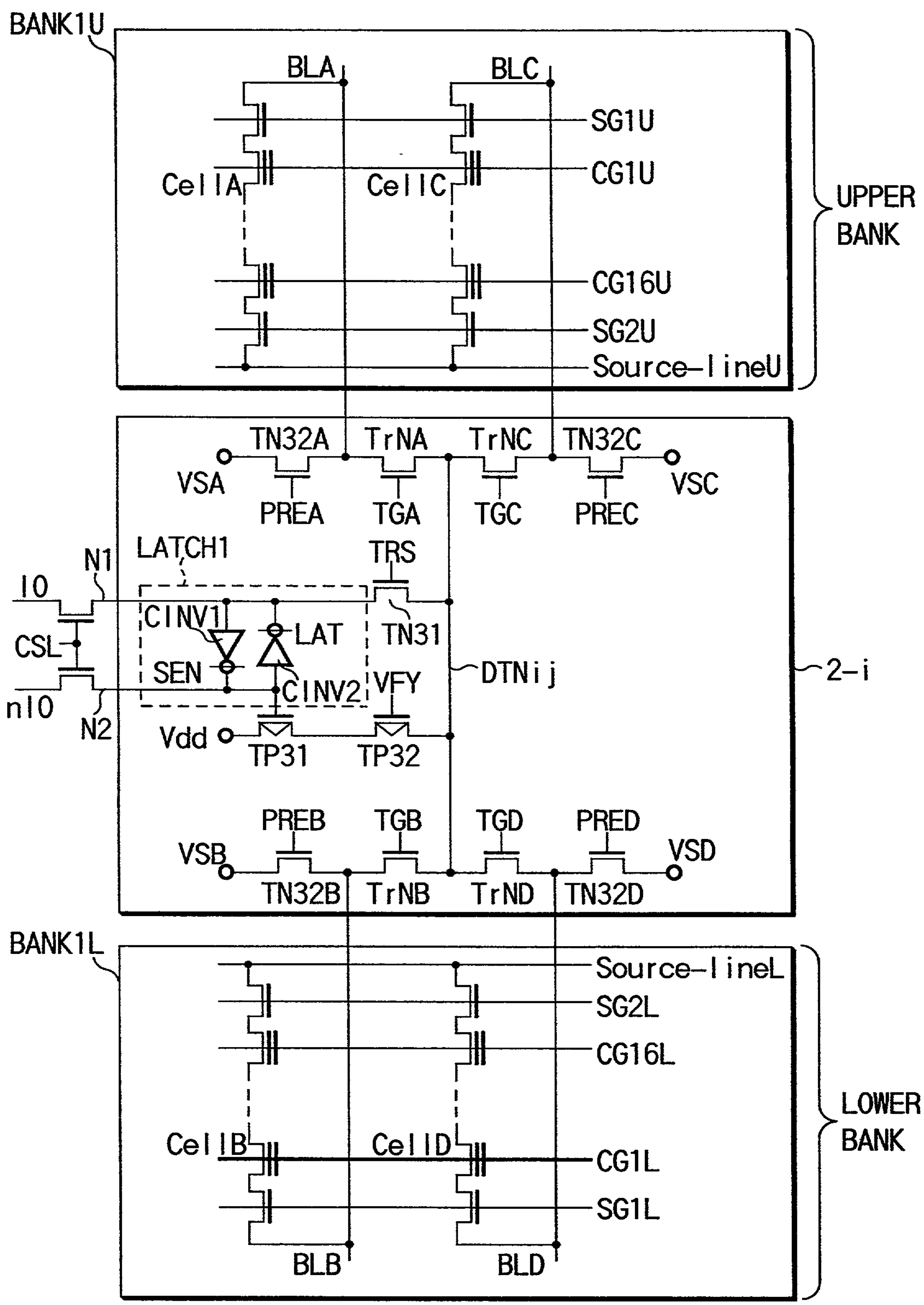

BANK1U
BLA
BLC
SG1U
CG1U
CellA
CellC
UPPER BANK
CG16U
SG2U
Source-lineU
TN32A
TrNA
TrNC
TN32C
VSA
VSC
PREA
TGA
TGC
PREC
N1
LATCH1
TRS
IO
CINV1
LAT
TN31
CSL
SEN
DTNij
2-i
CINV2
VFY
nIO
N2
Vdd
TP31
TP32
PREB
TGB
TGD
PRED
VSB
VSD
TN32B
TrNB
TrND
TN32D
BANK1L
Source-lineL
SG2L
CG16L
LOWER BANK
CellB
CellD
CG1L
SG1L
BLB
BLD

FIG. 62

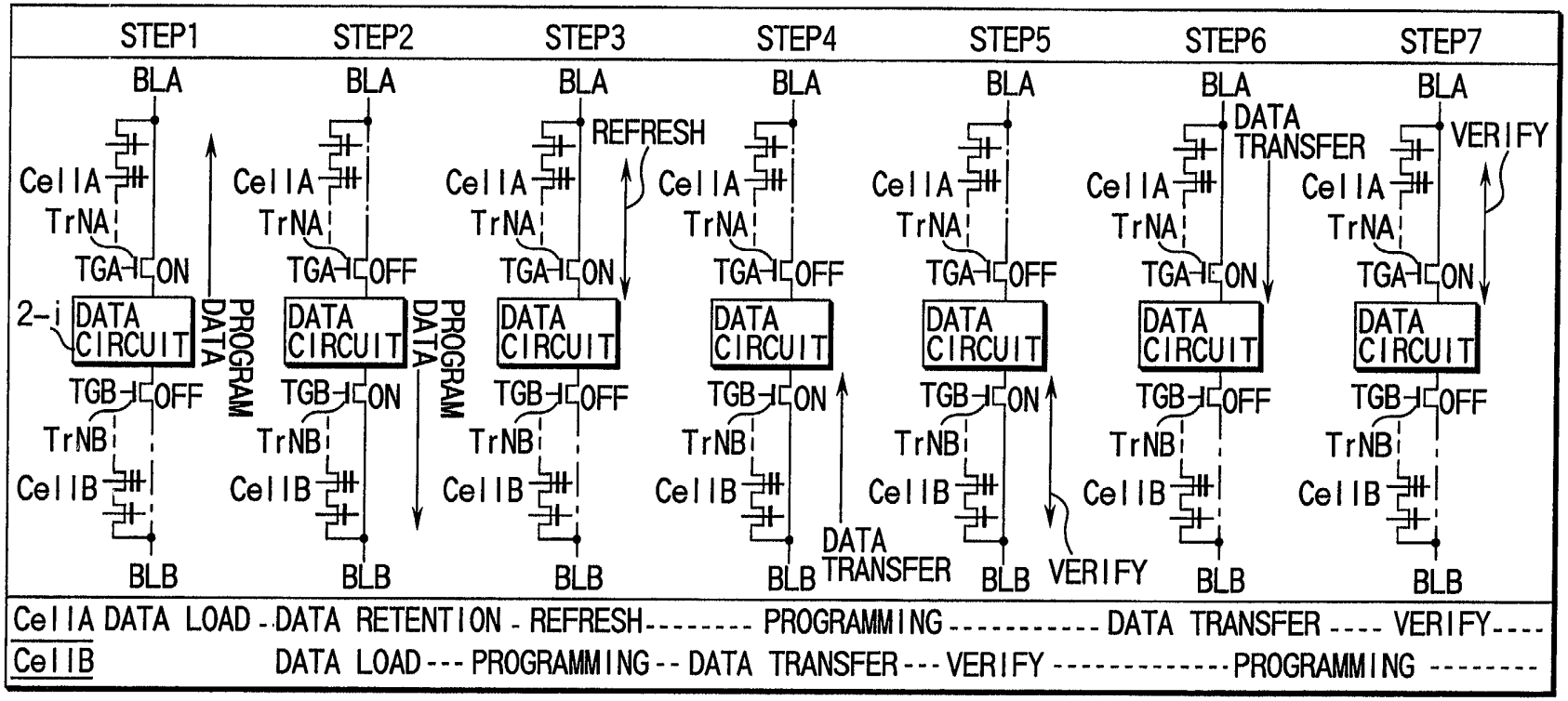

STEP1
STEP2
STEP3
STEP4
STEP5
STEP6
STEP7
BLA
CellA
TrNA
TGA
ON
OFF
2-i
DATA CIRCUIT
PROGRAM DATA
TGB
TrNB
CellB
BLB
REFRESH
DATA TRANSFER
VERIFY
CellA DATA LOAD - DATA RETENTION - REFRESH-------- PROGRAMMING ---------- DATA TRANSFER ---- VERIFY----
CellB DATA LOAD --- PROGRAMMING -- DATA TRANSFER --- VERIFY ---------- PROGRAMMING --------

FIG. 63

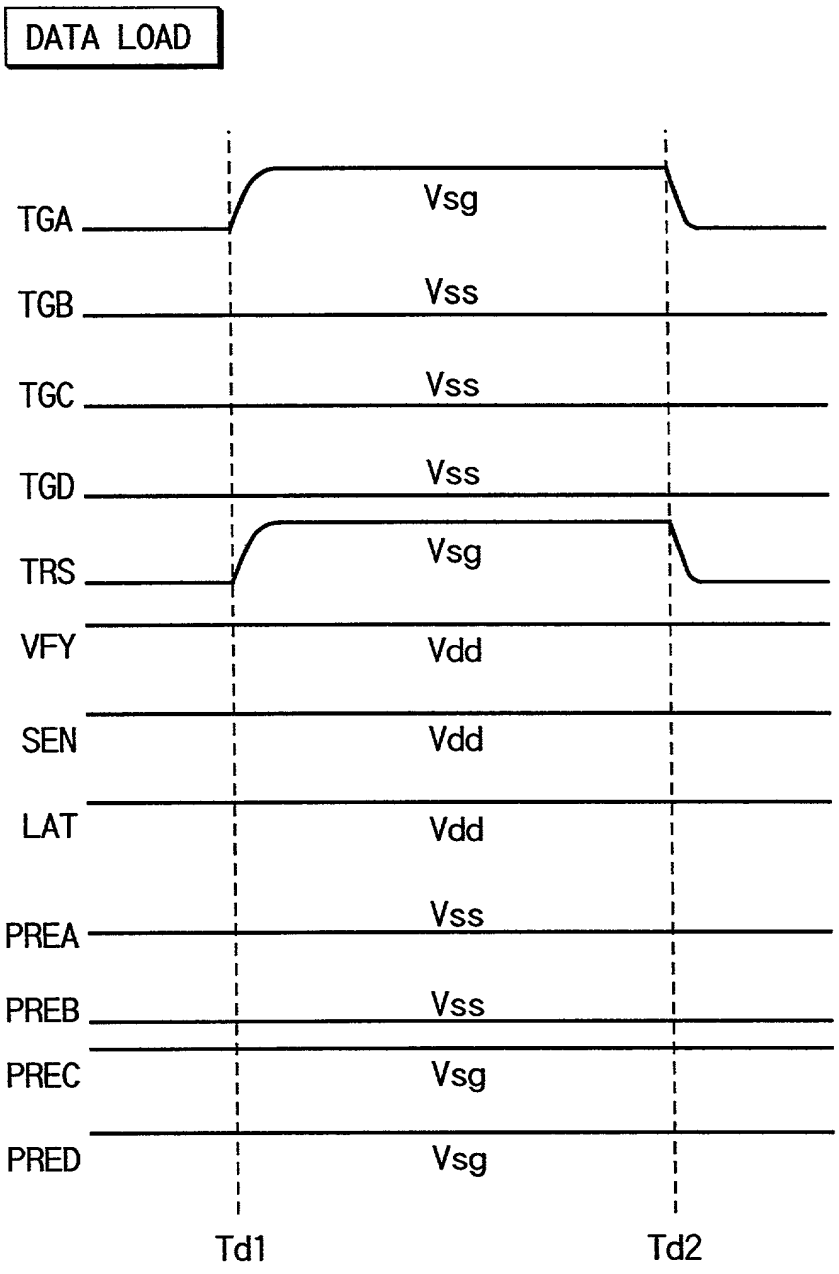


FIG. 64

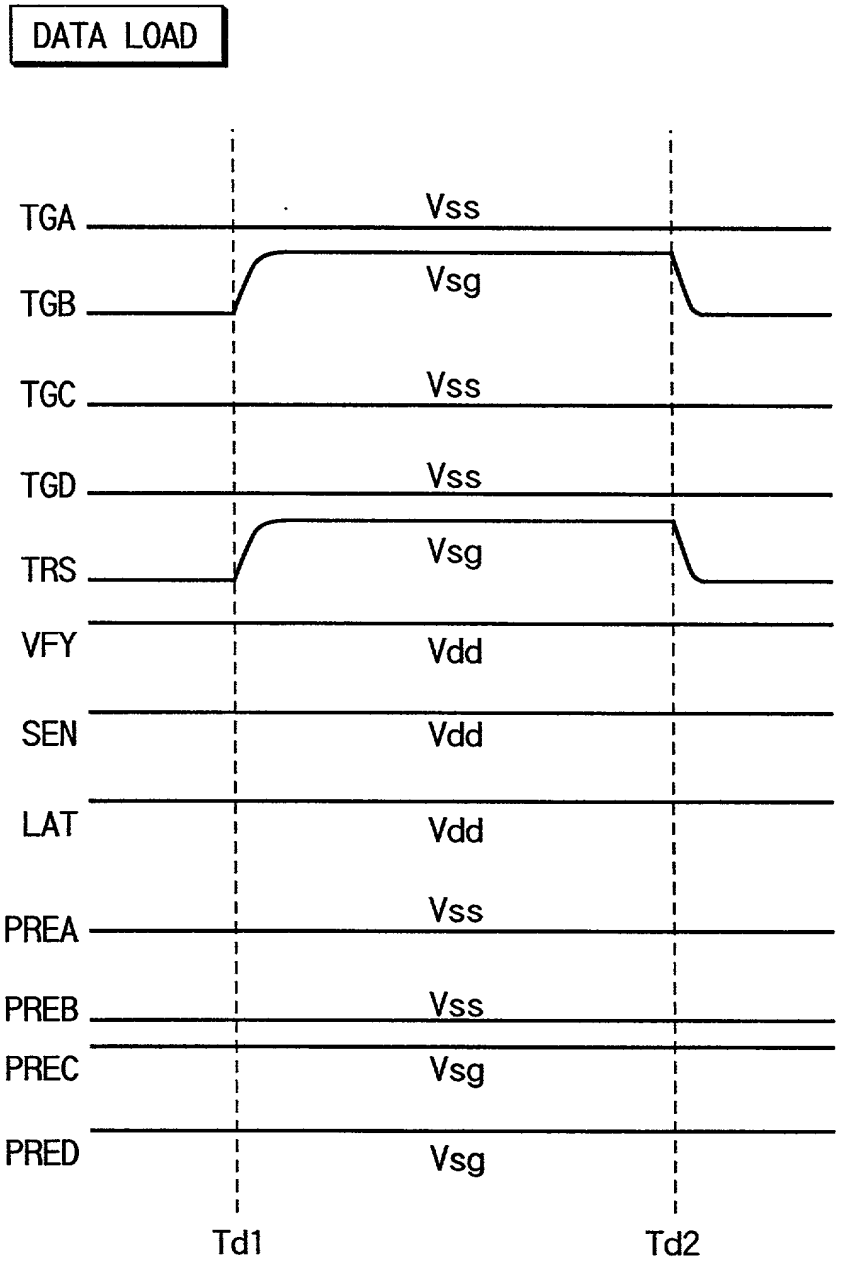
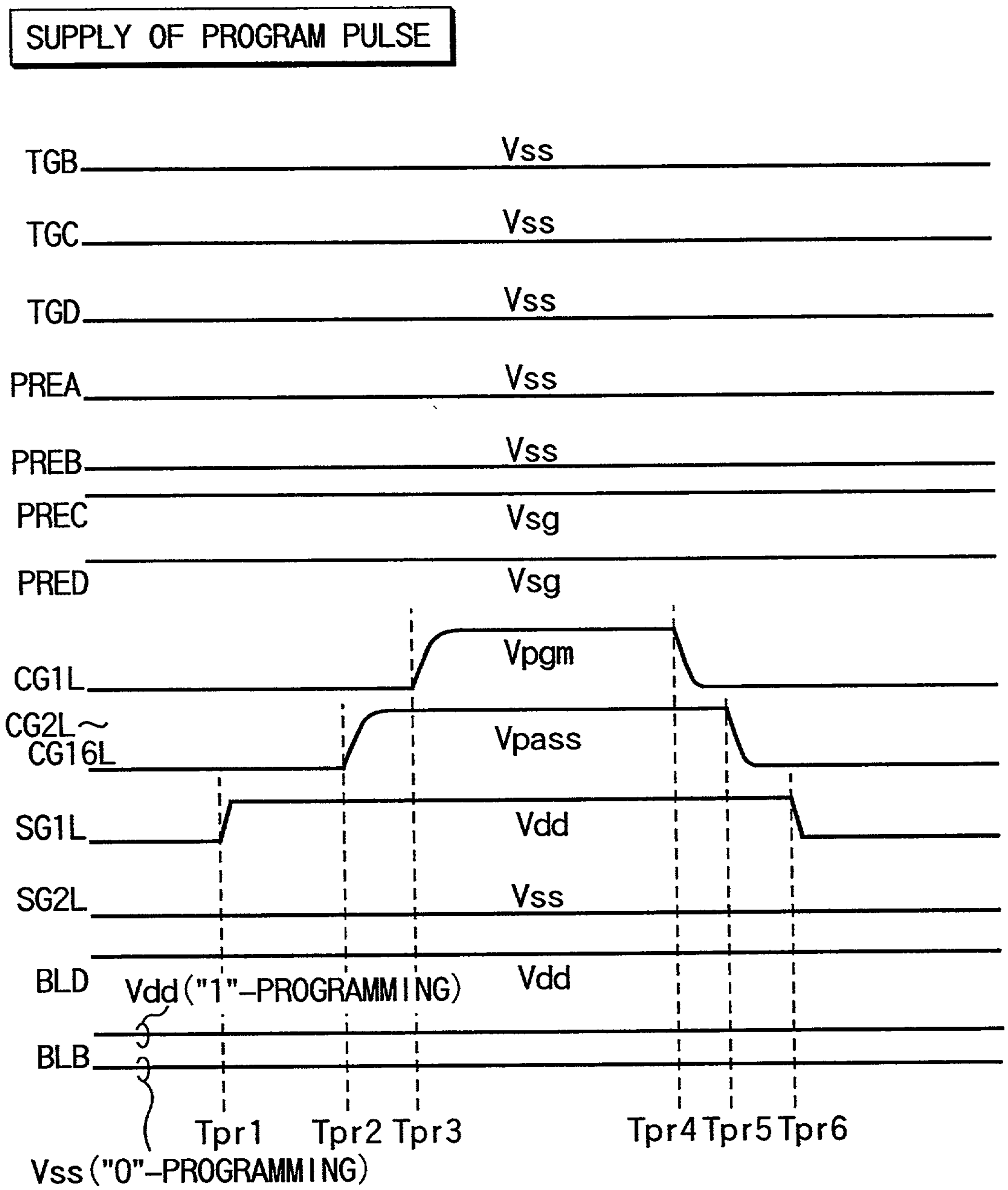
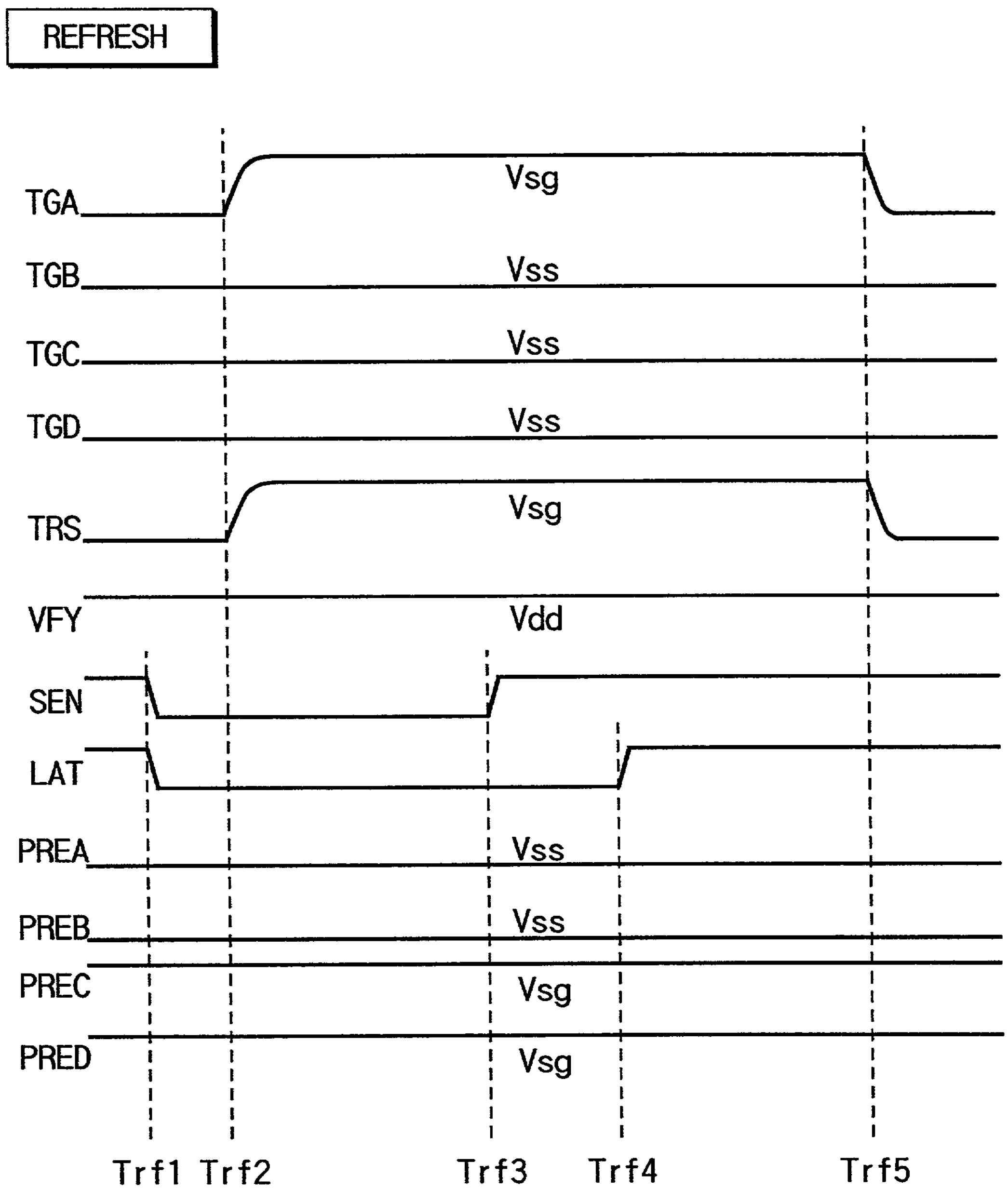


FIG. 65



SUPPLY OF PROGRAM PULSE
TGB
Vss
TGC
Vss
TGD
Vss
PREA
Vss
PREB
Vss
PREC
Vsg
PRED
Vsg
CG1L
Vpgm
CG2L~
CG16L
Vpass
SG1L
Vdd
SG2L
Vss
BLD
Vdd("1"-PROGRAMMING)
Vdd
BLB
Tpr1
Tpr2
Tpr3
Tpr4
Tpr5
Tpr6
Vss("0"-PROGRAMMING)

FIG. 66



REFRESH
TGA
Vsg
TGB
Vss
TGC
Vss
TGD
Vss
TRS
Vsg
VFY
Vdd
SEN
LAT
PREA
Vss
PREB
Vss
PREC
Vsg
PRED
Vsg
Trf1
Trf2
Trf3
Trf4
Trf5

FIG. 67

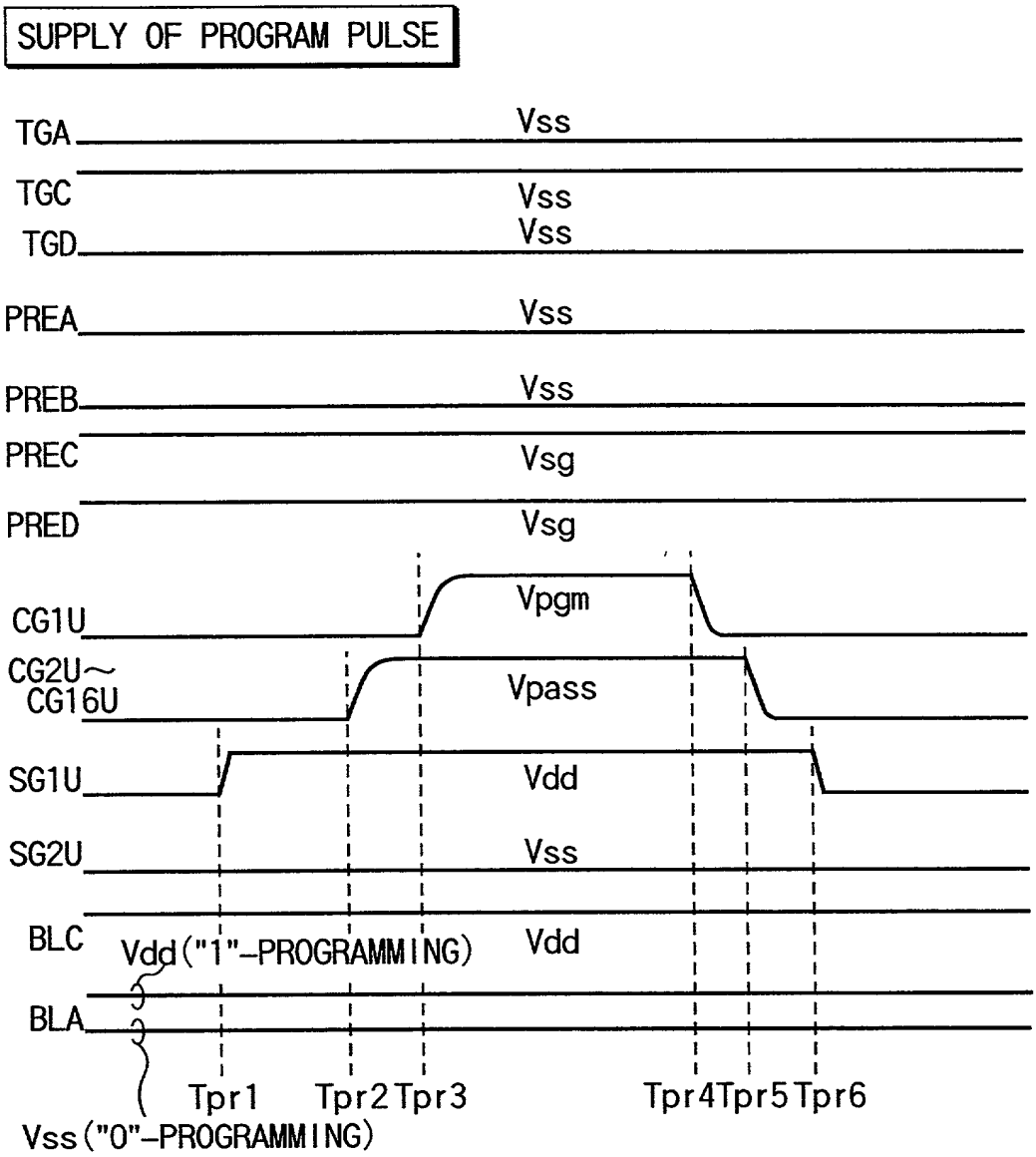
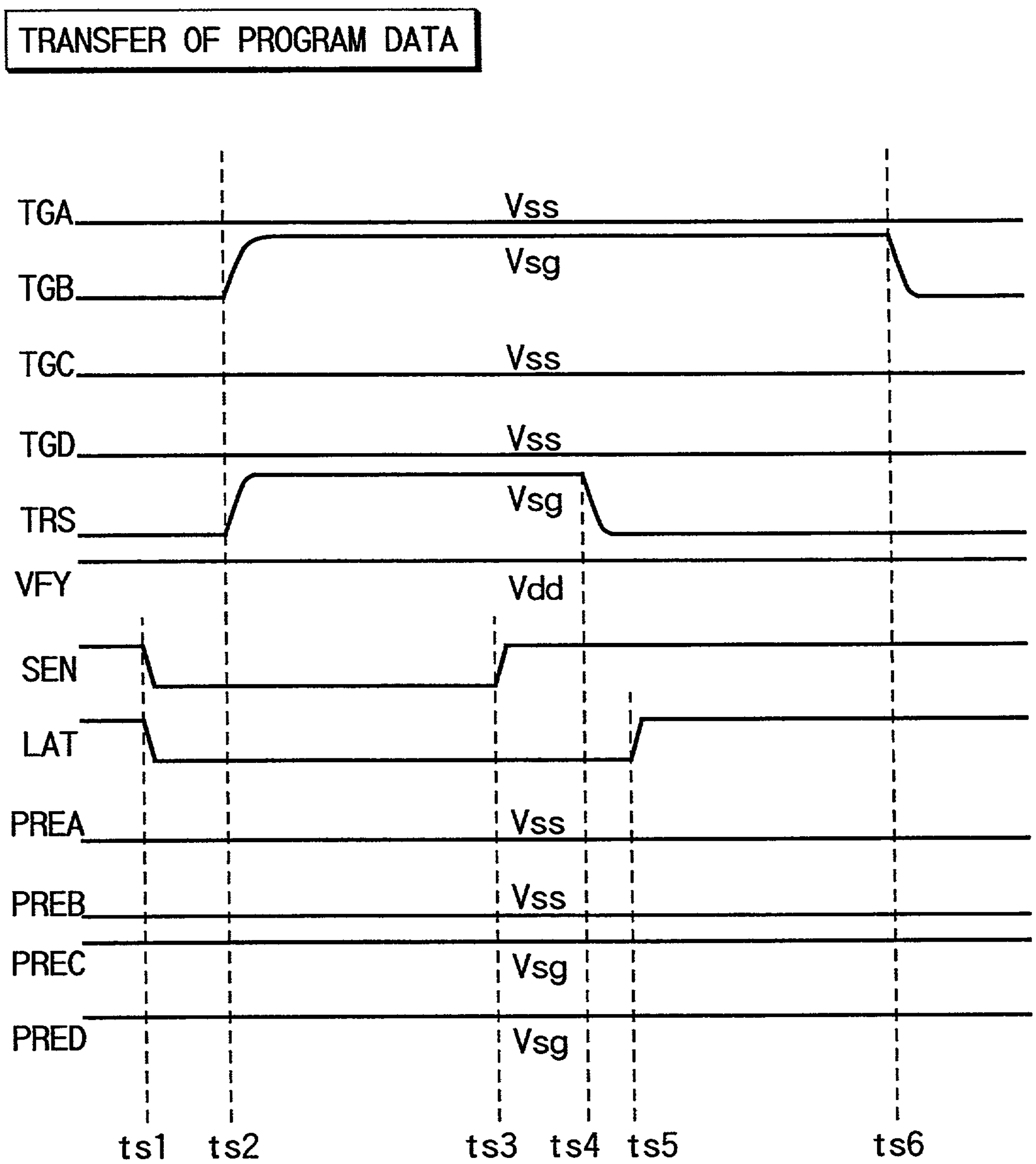


FIG. 68



TRANSFER OF PROGRAM DATA
TGA
TGB
TGC
TGD
TRS
VFY
SEN
LAT
PREA
PREB
PREC
PRED
Vss
Vsg
Vss
Vss
Vsg
Vdd
Vss
Vss
Vsg
Vsg
ts1
ts2
ts3
ts4
ts5
ts6

FIG. 69

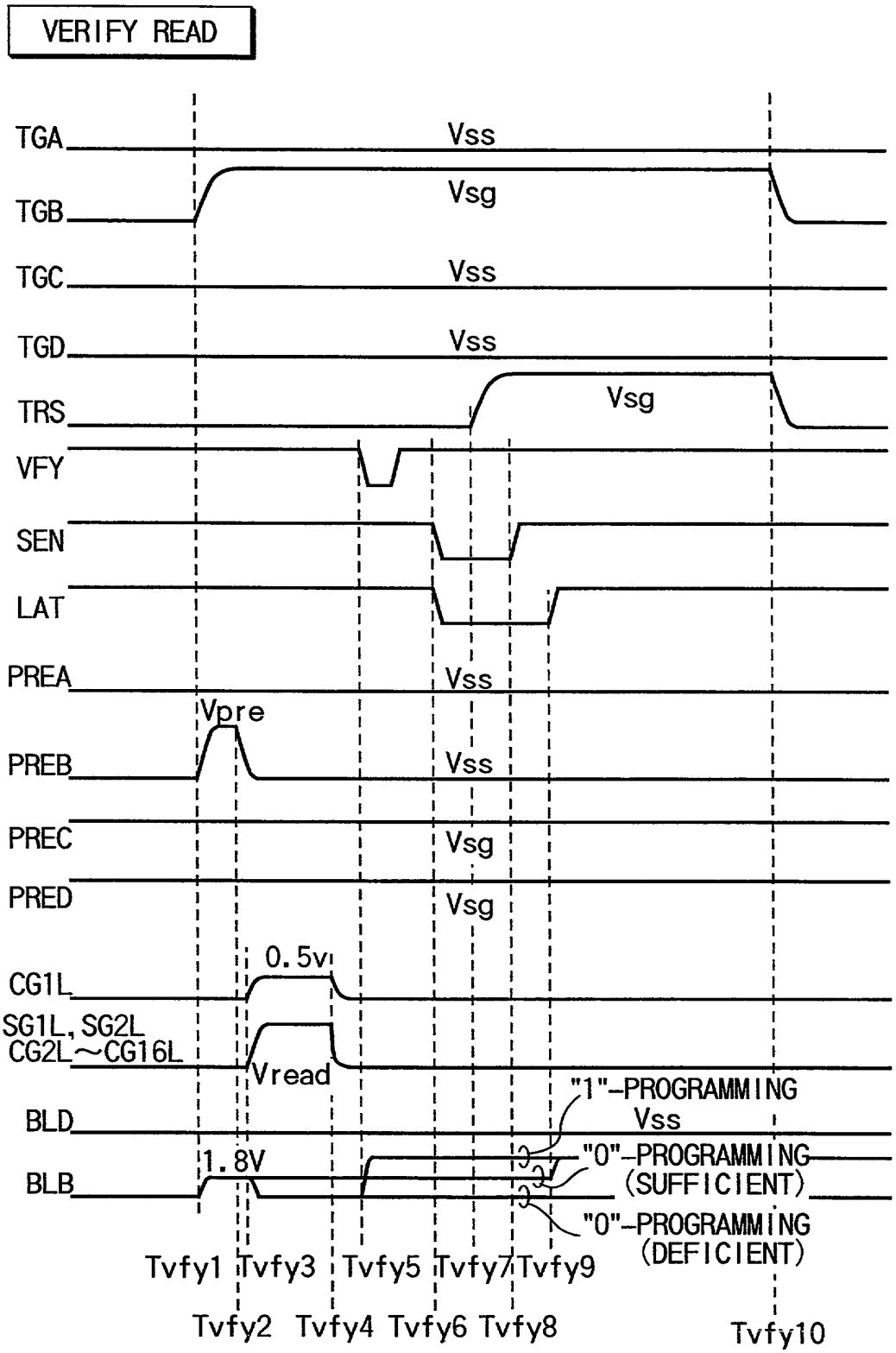

VERIFY READ
TGA
Vss
TGB
Vsg
TGC
Vss
TGD
Vss
TRS
Vsg
VFY
SEN
LAT
PREA
Vss
Vpre
PREB
Vss
PREC
Vsg
PRED
Vsg
0.5v
CG1L
SG1L, SG2L
CG2L~CG16L
Vread
"1"-PROGRAMMING
Vss
BLD
1.8V
"0"-PROGRAMMING
(SUFFICIENT)
BLB
"0"-PROGRAMMING
(DEFICIENT)
Tvfy1 Tvfy3 Tvfy5 Tvfy7 Tvfy9
Tvfy2 Tvfy4 Tvfy6 Tvfy8
Tvfy10

FIG. 70

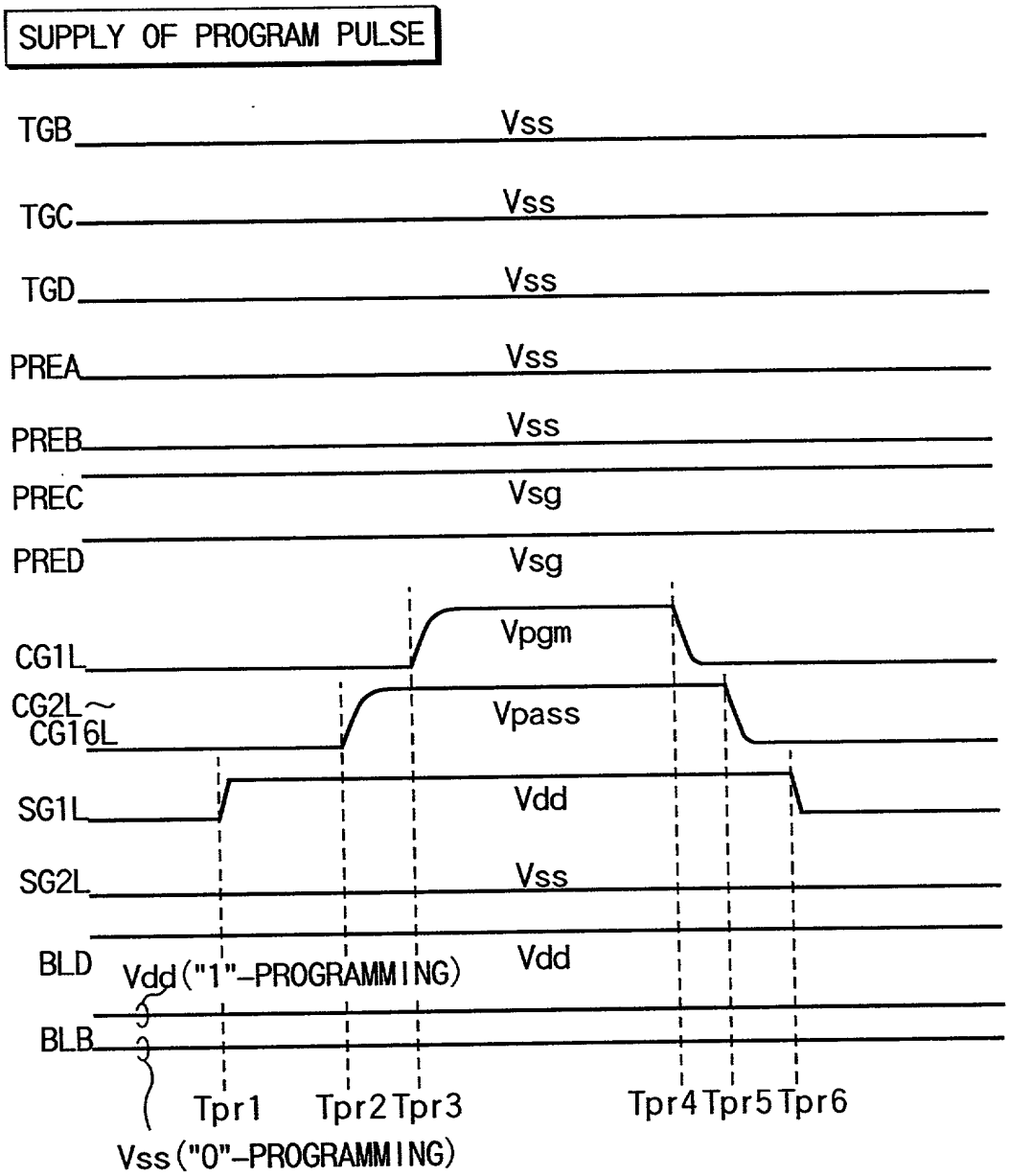

SUPPLY OF PROGRAM PULSE
TGB
Vss
TGC
Vss
TGD
Vss
PREA
Vss
PREB
Vss
PREC
Vsg
PRED
Vsg
CG1L
Vpgm
CG2L~
CG16L
Vpass
SG1L
Vdd
SG2L
Vss
BLD
Vdd("1"-PROGRAMMING)
Vdd
BLB
Vss("0"-PROGRAMMING)
Tpr1
Tpr2
Tpr3
Tpr4
Tpr5
Tpr6

FIG. 71

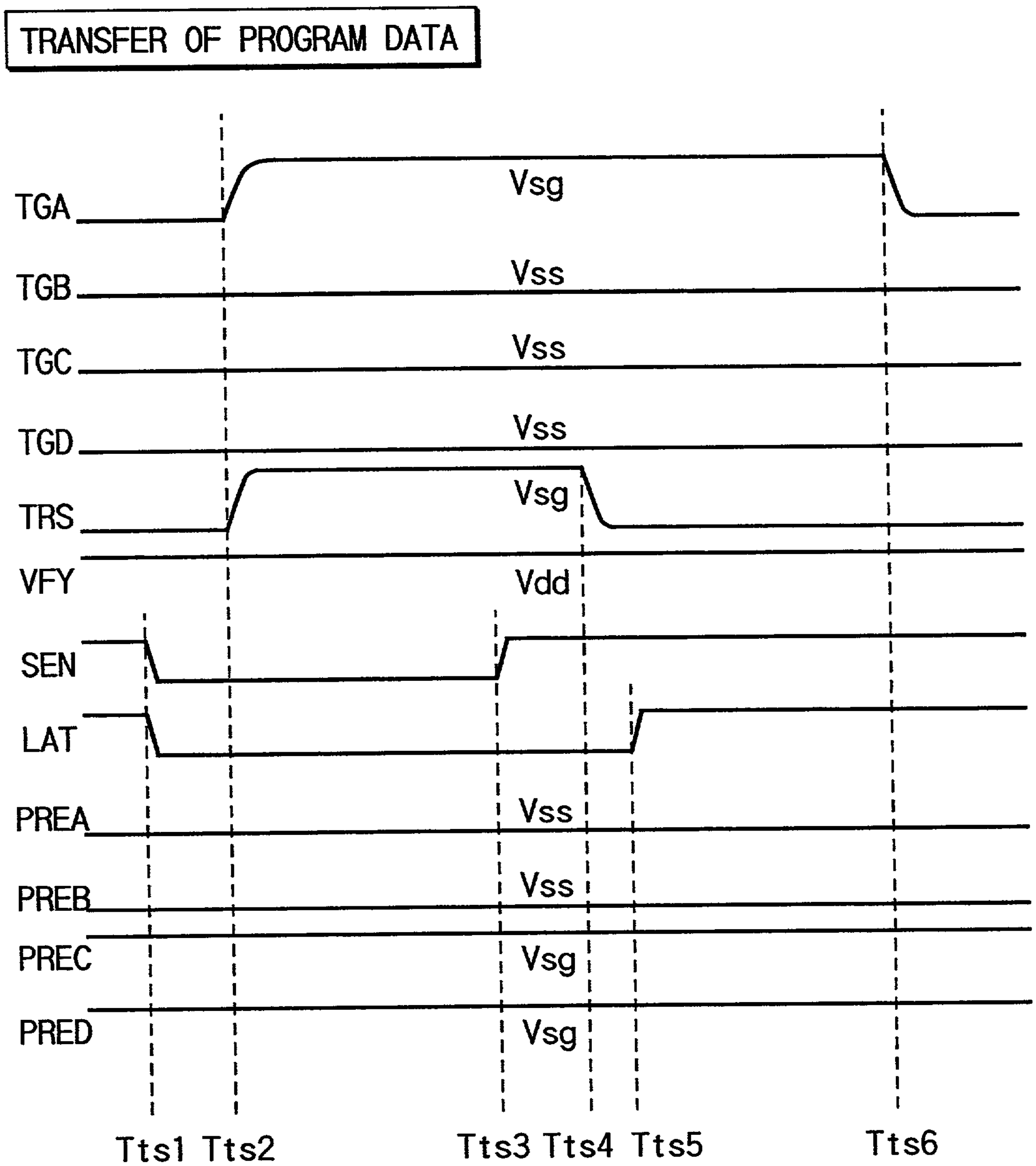

TRANSFER OF PROGRAM DATA
TGA
Vsg
TGB
Vss
TGC
Vss
TGD
Vss
TRS
Vsg
VFY
Vdd
SEN
LAT
PREA
Vss
PREB
Vss
PREC
Vsg
PRED
Vsg
Tts1
Tts2
Tts3
Tts4
Tts5
Tts6

FIG. 72

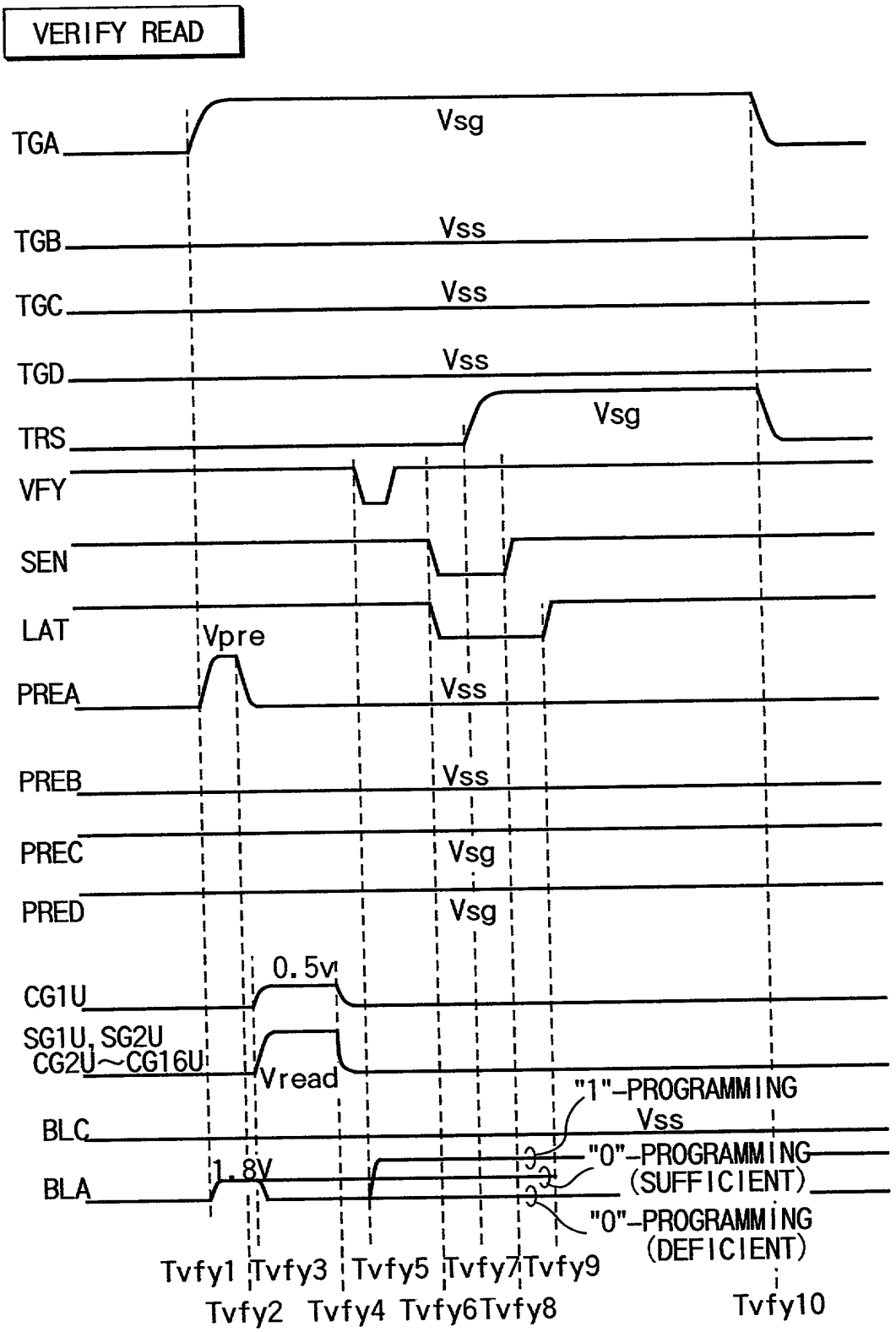


FIG. 73

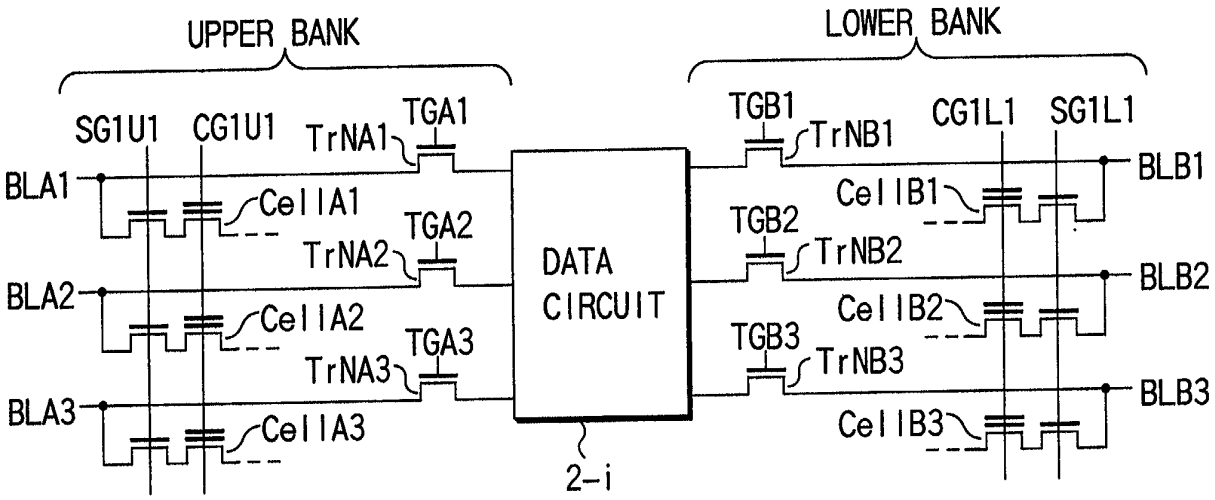

UPPER BANK
LOWER BANK
SG1U1
CG1U1
TrNA1
TGA1
BLA1
CellA1
TGA2
TrNA2
BLA2
CellA2
TGA3
TrNA3
BLA3
CellA3
DATA
CIRCUIT
2-i
TGB1
TrNB1
CG1L1
SG1L1
BLB1
CellB1
TGB2
TrNB2
BLB2
CellB2
TGB3
TrNB3
BLB3
CellB3

FIG. 74

	STEP1-1	STEP1-2	STEP1-3	STEP1-4	STEP1-5	STEP1-6	STEP1-7
TrNA1	ON	OFF	OFF	ON	OFF	OFF	OFF
TrNA2	OFF	ON	OFF	OFF	ON	ON	OFF
TrNA3	OFF	OFF	ON	OFF	OFF	OFF	OFF
TrNB1	OFF→ON	OFF	OFF	OFF→ON	OFF	OFF	ON
TrNB2	OFF	OFF→ON	OFF	OFF	OFF→ON	ON	OFF
TrNB3	OFF	OFF	OFF→ON	OFF	OFF	OFF	OFF
CellA1	DATA LOAD----	DATA RETENTION	-----REFRESH-------		PROGRAMMING---	DATA TRANSFER FROM BLB1 TO DL	
CellA2	——	DATA LOAD----	DATA RETENTION	---REFRESH--	PROGRAMMING---	DATA RETENTION	
CellA3	——	——	DATA LOAD----	DATA RETENTION	---PROGRAMMING---	DATA RETENTION	

DL : DATA LATCH (LATCH CIRCUIT IN DATA CIRCUIT)

FIG. 75

	STEP1-8	STEP1-9	STEP1-10	STEP1-11	STEP1-12
TrNA1	ON	OFF	OFF	OFF	OFF
TrNA2	OFF	OFF	ON	OFF	OFF
TrNA3	OFF	OFF	OFF	OFF	ON
TrNB1	OFF→ON	OFF	OFF	OFF	OFF
TrNB2	OFF	ON	OFF→ON	OFF	OFF
TrNB3	OFF	OFF	OFF	ON	OFF→ON
CellA1	VERIFY ----------		DATA RETENTION ----------		
CellA2	DATA RETENTION --	DATA TRANSFER FROM BLB2 TO DL	-- VERIFY -------	DATA RETENTION	-----
CellA3	DATA RETENTION	----------		DATA TRANSFER FROM BLB3 TO DL	--- VERIFY

DL : DATA LATCH (LATCH CIRCUIT IN DATA CIRCUIT)

FIG. 76

	STEP1-13	STEP1-14	STEP1-15	STEP1-16	STEP1-17
TrNA1	OFF	ON	OFF	OFF	OFF
TrNA2	OFF	OFF	OFF	ON	ON
TrNA3	OFF	OFF	OFF	OFF	OFF
TrNB1	ON	OFF	OFF	OFF	OFF
TrNB2	OFF	OFF	ON	OFF	ON
TrNB3	OFF	OFF	OFF	OFF	OFF
CellA1	DATA TRANSFER FROM BLB1 TO DL	DATA TRANSFER FROM DL TO BLA1	DATA RETENTION		PROGRAMMING
CellA2	DATA RETENTION		DATA TRANSFER FROM BLB2 TO DL	DATA TRANSFER FROM DL TO BLA2	PROGRAMMING
CellA3	DATA RETENTION				PROGRAMMING

DL : DATA LATCH (LATCH CIRCUIT IN DATA CIRCUIT)

FIG. 77

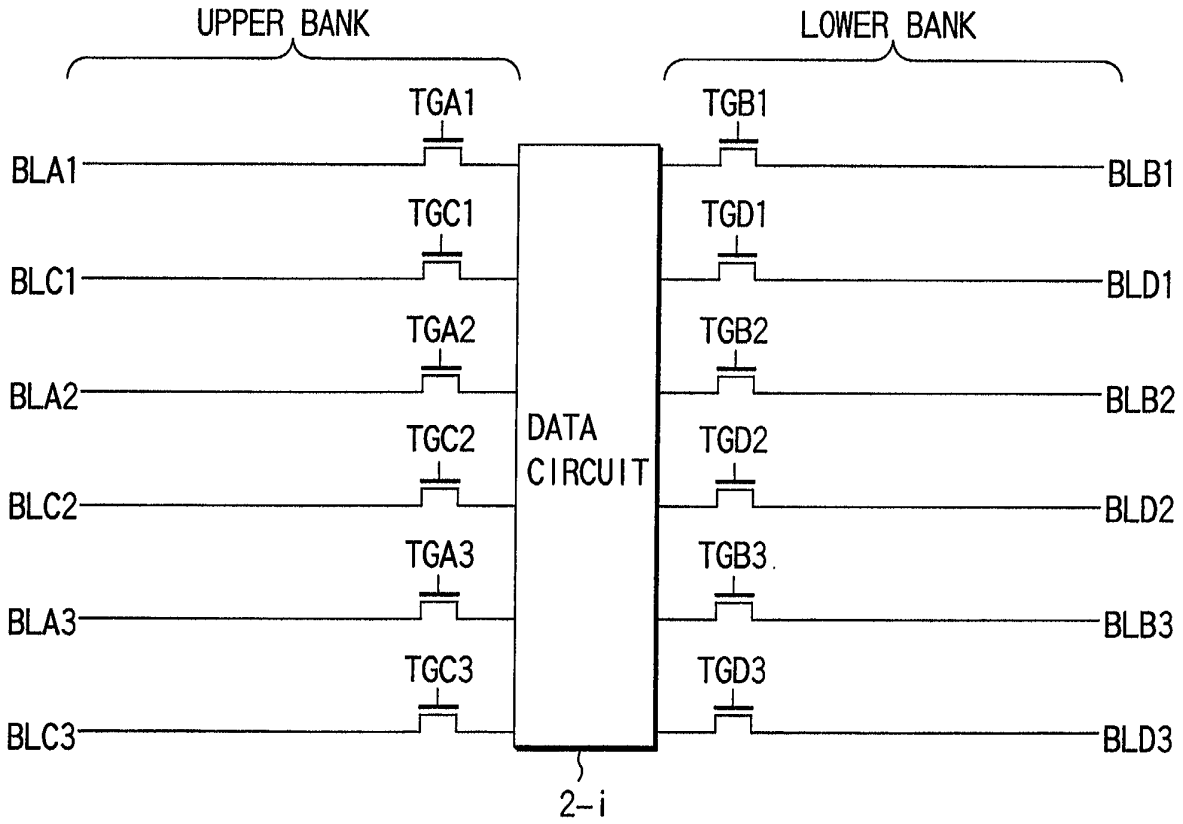

UPPER BANK
LOWER BANK
TGA1
TGB1
BLA1
BLB1
TGC1
TGD1
BLC1
BLD1
TGA2
TGB2
BLA2
BLB2
DATA
CIRCUIT
TGC2
TGD2
BLC2
BLD2
TGA3
TGB3
BLA3
BLB3
TGC3
TGD3
BLC3
BLD3
2-i

FIG. 78